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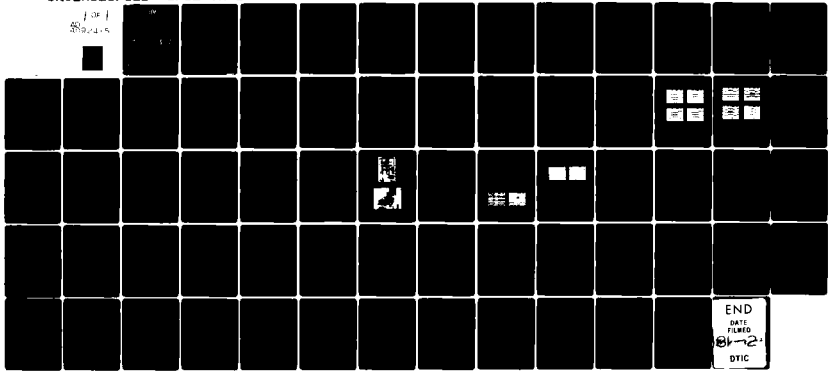

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RADIATION EVALUATION OF THE AM2901A MICROPROCESSOR

Bernd Deve

August 1980

Final Report

This research was sponsored by the Defense Nuclear Agency under Subtask Z99QAXTB029, Work Unit 62, Title: Radiation Characterization of MSI/LSI.

AIR FORCE WEAPONS LABORATORY
Air Force Systems Command
Kirtland Air Force Base, NM 87117

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This report has been reviewed by the Public Affairs Office and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations.

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Bit Slice	Dose Rate Upset	
TTL	Functional Tests	
Digital Circuit	Dynamic Tests	

20 ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This report describes the development of a program to perform a radiation evaluation and error analysis of the AM2901A bit-slice microprocessor. The integrated circuit (IC) manufacturer's functional and dynamic test sets were obtained and rewritten using algorithmic pattern generation programming techniques to run on an in-house MD-104 tester. The test procedure and radiation evaluation of the microprocessor are presented. The devices were tested in neutron, total gamma dose, and transient ionizing dose-rate environments.

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CONTENTS

I. INTRODUCTION

The purpose of this program was to determine methods for in-house testing of microprocessors that could be used for radiation evaluation of microprocessors. Besides determining the failure threshold of a microprocessor in various radiation environments, the tests should also be able to isolate faults so that recommendations can be made to improve the radiation response.

Techniques for testing microprocessors are considerably more complex than those for testing other large-scale integration (LSI) devices such as memories, since memory chips have very structured architecture allowing straightforward evaluation using standard test routines such as checkerboard, walking ONE and ZERO, and galloping ONE and ZERO PATTERNS. Memory tests are designed to check for proper cell operation plus possible interaction between cells (pattern sensitivity) and these tests are valid for all memories regardless of size. Problems that make microprocessor testing more difficult include significant differences in device architecture, instruction sets, bus organization, input/output capabilities, various bit sizes, and large package size (pin count). Due to the above mentioned variations among microprocessors, the testing technique is different for every microprocessor, although the basic approaches may be similar for a given set of devices.

Section II briefly describes some of these common microprocessor testing techniques. This is followed by the test procedure used for the in-house radiation evaluation of Advanced Micro Device AM2901A using a Macrodata MD-104 tester.

Section III covers the radiation test procedures and the radiation response data. Twenty-one devices were exposed to neutron, total gamma dose, and transient ionizing radiation environments.

II. 2901A ELECTRICAL CHARACTERIZATION

A variety of techniques exist for functional testing of microprocessors. The most common of these include the self-diagnostic method, comparison method, algorithmic pattern generation, and stored response testing (Ref. 1). These techniques vary in terms of comprehensiveness of the evaluation, software development time, and cost and complexity of the tester required.

The self-diagnostic method usually consists of running an application oriented program on the microprocessor in its intended operating environment. This results in inexpensive testing in a real environment, but provides very little data other than simple go/no-go functional information.

In the comparison method of testing, identical inputs are applied in parallel to the device under test (DUT) and a "known good device." The outputs are compared and, if the signals from both devices match, the device under test is considered good. This method requires little mass memory since the output need not be stored; it also allows real-time functional testing and is relatively easy to implement. Drawbacks are defining a known good device, being limited to speed and timing constraints of the reference device, and having no parametric measurements; also, this approach is not likely to detect logic, design, or documentation errors.

Algorithmic pattern generation consists of developing algorithms to apply input patterns to the device under test. Expected outputs can also be produced by algorithms, so long as the test patterns have some repetitive structure. This test technique also requires a minimum of mass memory, and is flexible enough to allow the user to perform some fault diagnosis through program alterations. Some disadvantages are that (1) it is difficult to generate non-algorithmic patterns, and (2) test programs can become complex and must be implemented in low level language. Testers of this type generally are not complex enough to allow parametric testing.

The stored response method can be implemented with a predicted pattern or learned pattern. The learned output is obtained by applying the input set to a known good device and then saving this output in memory. The predicted output is determined by logic or functional simulaton. Logic simulation requires a

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1. Scrupski, S. E., "Why and How Users Test Microprocessors," Electronics, pp. 97-104, March 2, 1978.

correct circuit schematic and a significant implementation effort but will result in a short efficient pattern that will cover most of the device's circuit nodes. Functional simulation proves the device performs the documented functions, but also requires a significant implementation effort. All input and output responses are saved in memory. Testers of this complexity also perform dynamic and parametric measurements but are expensive.

The most applicable in-house tester available for microprocessor evaluations was a Macrodata MD-104. This is a processor controlled, 10 MHz test system with a 256 x 24-bit program memory, a 256 x 16-bit data buffer memory (DBM), and several accessible address, data, and loop control registers. It is primarily intended as a memory test system using algorithmically generated patterns to test the memory. Thus the approach available to test a microprocessor is basically limited to pattern generation of the input test set and corresponding output.

Of the microprocessors available in mid-1977, Advanced Micro Device's 2901A bipolar 4-bit slice and RCA's 1802 CMOS 8-bit microprocessor were of most interest since both of these technologies appeared to have military system applications. Preliminary investigation into writing programs for testing these devices resulted in choosing the AM2901A for radiation evaluation. The primary reason was that the 2901A is a 4-bit machine and therefore has fewer data input/output ports and address lines. This was important since the MD-104 DBM word length is 16 bits and most 1802 test instructions would require multiple MD-104 words to contain the input, output, and address data, whereas this could be accomplished in one word using the 2901A. The 1802 would therefore require a considerably longer program than that for the 2901A. Since the MD-104 contains limited memory, the fewer words required for each test, the more comprehensive the test progrram could be.

Following the decision to radiation evaluate the 2901A, a test set needed to be developed. Since the purpose of the project was to perform a radiation evaluation of the device and not do a complete electrical characterization spending a miminal amount of time developing the test set for device evaluation and failure analysis was desirable. A computer printout was obtained from Advanced Micro Devices listing the functional tests used by the manufacturer for verification of operational 2901A microprocessors. This test set included approximately 5000 functional tests with the corresponding output and 26

propagation delay tests. It appeared comprehensive enough for our needs and simple enough for implementation using the MD-104 tester. MD-104 programs were written to algorithmically generate the required input and output patterns. Software to perform the 5000 functional and 26 propagation delay tests used the entire MD-104 program memory space and data buffer memory. The DBM was used for storage of central processing unit (CPU) instructions, input/output patterns too random to generate by other methods, and internal AM 2901A RAM register data for the propagation delay tests.

A modular testing approach was taken by the vendor, whereby functional blocks within the 2901A (i.e., random access memory (RAM) registers, Q register, arithmetic logic unit (ALU), shift registers, ALU source and function selector) are tested in a specific order. Figure 1 shows a functional block diagram of the 2901A. The purpose behind modular testing is that, since it is impossible to test all internal paths with every data combination, the task of testing is simplified by thoroughly exercising each functional subsystem or module as a separate unit. The order of the testing is important because the next module to be tested often relies upon correct data from the previous module tested. As an example, the RAM register outputs are inputs to the ALU data source selector; therefore, the RAM is checked with a galloping ONEs and ZEROs pattern to verify proper operation so that good RAM data will be transmitted to the ALU data source selector.

The following is a brief description of the 12 sets of functional tests. To aid in the description of the tests, Figures 1 and 2 (Ref. 2) show block diagrams of the microprocessor, and Figure 3 (Ref. 3) describes the instruction set.

1. The first 512 tests exercise the two-port RAM with addresses coming from the A port and data going through the ALU. A galloping ONE in a field of ZEROs pattern is used with a read OP code (1_8 - 1_0) of 134 and a write OP code of 337 (all OP codes are given in octal). The shift operation pins Q_0, Q_3, RAM_0, and RAM_3 are ignored during these first six sets of RAM tests. A galloping ONEs and ZEROs pattern tests all the bits, the addressing, interaction between bits, and

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2. McCaskill, Richard, "Wring Out 4-bit Microprocessor Slices", Electronic Design, 10 May 77, pp. 74-77.

3. AM 290Q Bipolar Microprocessor Family Data Book, Advanced Micro Devices, Inc., Sunnyvale, CA., 1976, p. 8.

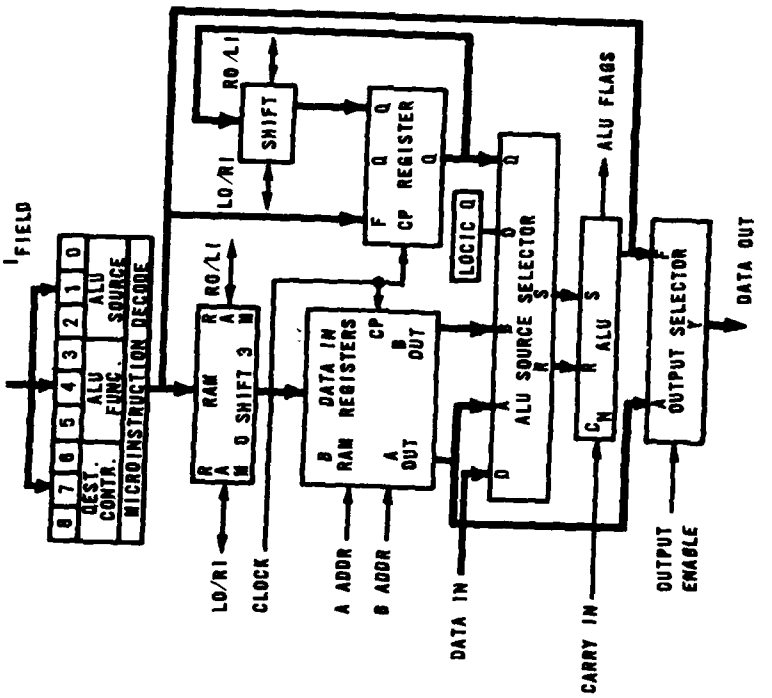


Figure 1. AM2901A functional block diagram (Ref. 2)

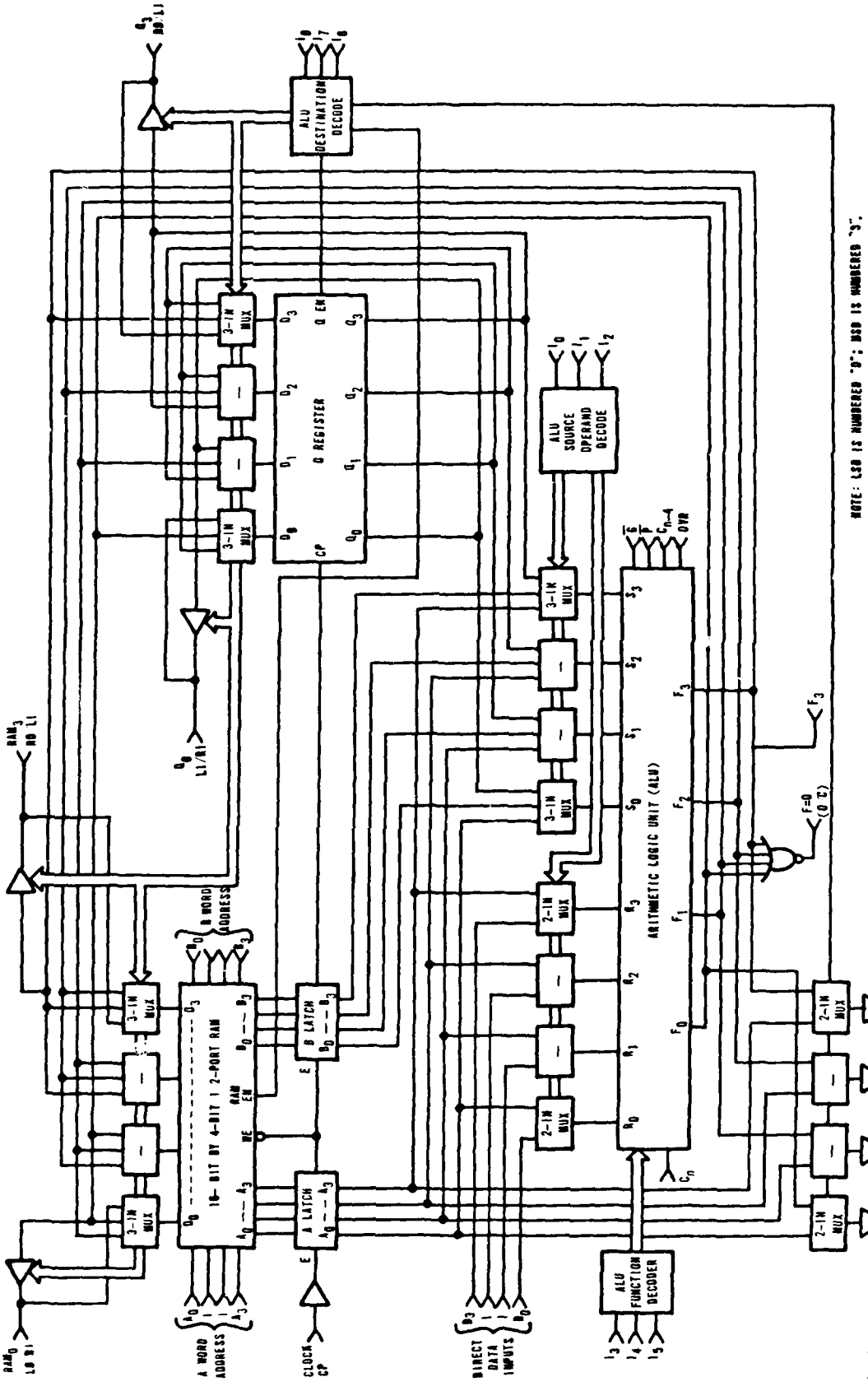


Figure 2. Detailed AM2901A block diagram (Ref. 2)

MICRO CODE				ALU SOURCE OPERANDS	
1_2	1_1	1_0	Octal Code	R	S
L	L	L	0	A	0
L	L	H	1	A	B
L	H	L	2	0	0
L	H	H	3	0	R
H	L	L	4	0	A
H	L	H	5	D	A
H	H	L	6	D	0
H	H	H	7	D	0

(a) ALU source operand control

MICRO CODE				ALU Function	Symbol
1_5	1_4	1_3	Octal Code		
L	L	L	0	R Plus S	R + S
L	L	H	1	S Minus R	S - R
L	H	L	2	R Minus S	R - S
L	H	H	3	R OR S	R V S
H	L	L	4	R AND S	R S
H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ S
H	H	L	6	R EX-OR S	$\underline{R \quad S}$
H	H	H	7	R EX-NOR S	R S

(b) ALU function control

Figure 3. Definition of microinstruction (1_8-1_0) code (Ref. 3).

MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 →	F	F_0	IN_3	Q_0	IN_3
H	L	H	5	DOWN	F/2 → B	X	NONE	F	F_0	IN_3	Q_0	X
H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_3	IN_0	Q_3
H	H	H	7	UP	2F → B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three state output which is in the high impedance state.

B = Register addressed by B inputs.

Up is toward MSB, Down is toward LSB.

(c) ALU destination control.

Figure 3. Continued

I_{210} OCTAL	0	1	2	3	4	5	6	7
OCTAL 543 / ALU Source / ALU Function	A,Q	A,B	0,Q	0,B	0,A	D,A	D,Q	D,0
0 — C_n = L R Plus S C_n = H	A+Q A+Q+1	A+B A+B+1	Q Q+1	B B+1	A A+1	D+A D+A+1	D+Q D+Q+1	D D+1
1 — C_n = L S Minus R C_n = H	Q-A-1 Q-A	B-A-1 B-A	Q-1 Q	B-1 B	A-1 A	A-D-1 A-D	Q-D-1 Q-D	-D-1 -D
2 — C_n = L R Minus S C_n = H	A-Q-1 A-Q	A-B-1 A-B	-Q-1 -Q	-B-1 -B	-A-1 -A	D-A-1 D-A	D-Q-1 D-Q	D-1 D
3 — R OR S	AVQ	AVB	Q	B	A	DVA	DVQ	D
4 — R AND S	A Q	A B	0	0	0	D A	D Q	0
5 — $\overline{R}$ AND S	$\overline{A}$ Q	$\overline{A}$ B	Q	B	A	$\overline{D}$ A	$\overline{D}$ Q	0
6 — R EX-OR S	A Q	A B	Q	B	A	D A	D Q	D
7 — R EX-NOR S	$\overline{A\ Q}$	$\overline{A\ B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D\ A}$	$\overline{D\ Q}$	$\overline{D}$

+ = Plus; - = Minus: V = OR and; = EX-OR

(d) Source operand and ALU function matrix.

Figure 3. Concluded

pattern and sequence dependencies. A test word is written in the first location, followed by writing the rest of the memory with the test word complement. The entire RAM is then read in the following sequence: background location, test word, next background location, test word, etc. Each succeeding location is checked in the same manner.

The next set of 512 tests also performs the same tests as in set 1, using the B address port instead of the A port. The read OP code is correspondingly changed to 133.

3. This set of 512 tests also performs a galloping ONE in a field of ZEROs test using the A address port. This time, however, the data are transferred directly to the Y output, bypassing the ALU. The write OP code is 337, while the read OP code is 233.

4-6. These three sets of tests are identical to sets 1-3 except that the galloping pattern is reversed. It is now a galloping ZERO in a field of ONEs.

7. These 16 tests check the ALU source code. The RAM and Q registers are preloaded with known values. Then with an ALU destination OP code of 1 (NO OP) and an ALU function code of 6 (exclusive OR), the source code is cycled from 0 to 7. The function code is then changed to 7 (exclusive NOR) and the source code is cycled through the sequence once more.

These 270 tests check the ALU functon code. During these tests, the memory is preloaded with content equal to the address. Then with A address equal to the B address, a destination OP code = 1 (NO OP) and source code = 1 (A and B ports selected), the ALU function code is cycled through the sequence of 7,5,4,0,1,3,2,6 for every set of A and B addresses. This whole process is then repeated with A address equal to the inverse of the B address.

9. These 530 tests check the arithmetic operation and carry generation. The memory is preloaded with content equal to the address location. With OP code 105, whereby the D input is added to the A port of memory, the tester cycles through every possible D input added to every word in memory with the input carry being both 0 and I.

10. These 512 tests check the Q register operation. During these tests, the Q register is first loaded with all zeros. Then with the carry input at zero (Cn = 0) and with OP code 006, whereby the Q register is loaded with the sam of data input and Q register content on every clock cycle, the device is

clocked through all possible data inputs. The carry input is then changed to a ONE, and with OP code 016 whereby the Q register is loaded with the difference of Q - D, the device is clocked through all possible data inputs again. This checks both the add and subtract modes of the ALU, the internal-carry-lookahead circuitry, and the Q register operation.

11. Those 84 tests are designed to check the Q register shifting. During these tests, a unique string of data (11100001010011011110) is shifted into the appropriate shift inputs. OP codes used in this group of tests are 432 for shift left, 532 for no shift, 632 for shift right, and 732 for no shift.

12. The final set of 84 tests check for proper RAM shift operation. During these tests, the A and B addresses are set at word 0. The same string of data as in test set 11 is shifted into the appropriate shift inputs. OP codes 434 and 533 are used for left shifts, and codes 634 and 733 for right shifts.

Besides these functional tests, a set of 26 dynamic tests (also received from Advanced Micro Devices) was performed. These dynamic tests use different instructions (many requiring preloading of the RAM and Q registers) to measure the propagation delay times from various inputs such as RAM addresses, data input, carry input, RAM shift input, and Q shift input to the output ports (Y3-Y0) and status flags. The MD-104 is not equipped to make these types of dynamic measurements, but programs were written to preload the 2901A and execute the necessary instructions to measure the propagation delays. The MD-104 program then continually loops the given set of instructions until the propagation delay between the input and output can be measured on an oscilloscope. A switch is then manually depressed which causes the MD-104 to automatically loop the next of the 26 dynamic tests. To increase the testing throughput and eliminate the possibility of connecting the scope probes to the wrong input or output pins, the inputs and outputs used in these dynamic tests were multiplexed. That is, one multiplexer set would contain the correct 2901A input for the 26 tests, and another multiplexer set would contain the corresponding output to be measured. Generally, several different propagation delays can be measured off of one input, so there are actually two sets of multiplexed outputs. For example, during an ADD instruction the propagation delay can be measured between the data input bit 0 (D0) and output bit 0 (Y0), and also between D0 and the carry output (Cn + 4). Table 1 is a sample of the dynamic tests showing the input and output pins measured and the typical propagation delay times of the

TABLE 1. AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: *** TYPICAL SPECS *** NO. OF DEVICES: 1

TEST NO.	INPUT	OUT1 (nS):	tPd0	tPd1	OUT2 (nS):	tPd0	tPd1
1	D0	Y0	45.0	45.0	Y3	45.0	45.0
2	D3	G'	35.0	35.0	OVR	55.0	55.0
3	Cn	RAM0	50.0	50.0	RAM0	.0	.0
4	I0	Y1	55.0	55.0	F3	55.0	55.0
5	I0	G'	45.0	45.0	OVR	65.0	65.0
6	D0	RAM0	60.0	60.0	RAM0	.0	.0
7	I5	Y0	55.0	55.0	Y2	55.0	55.0
8	I5	RAM0	75.0	75.0	RAM0	.0	.0
9	I5	Cn+4	55.0	55.0	Cn+4	.0	.0
10	I4	F=0	70.0	70.0	F3	55.0	55.0
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	30.0	30.0	RAM3	30.0	30.0
13	CLK	Q0	30.0	30.0	RAM0	80.0	80.0
14	CLK	Y0	60.0	60.0	Y0	60.0	60.0
15	CLK	Cn+4	60.0	60.0	Cn+4	60.0	60.0
16	A0	Y0	45.0	45.0	Y2	45.0	45.0
17	A3	Y1	45.0	45.0	Y3	45.0	45.0
18	B0	Y0	80.0	80.0	P'	65.0	65.0
19	A0	Y2	80.0	80.0	Cn+4	65.0	65.0
20	B2	G'	65.0	65.0	OVR	85.0	85.0
21	A2	G'	65.0	65.0	OVR	85.0	85.0
22	Cn	OVR	30.0	30.0	OVR	.0	.0
23	Cn	Y0	30.0	30.0	Cn+4	20.0	20.0
24	I8	Y3	30.0	30.0	Y1	30.0	30.0
25	CLK	Y1	60.0	.0	F=0	75.0	.0
26	CLK	Y3	60.0	.0	F3	60.0	.0

POWER SUPPLY CURRENT (Icc) = 160.0 mA

OUTPUT SINK CURRENT : Y0 I(OL) = 20.0 mA Cn+4 I(OL) = 1.6 mA
OUTPUT SOURCE CURRENT: Y0 I(OH) = 10.0 mA Cn+4 I(OH) = 1.0 mA

AM2901A. $T_{pd}0$ is the propagation delay time required for the output to go to a ZERO state for a given change in the input, while $T_{pd}1$ is the time required for the output to get to a ONE state. Certain tests such as 3, 6, 8, and 9 have only one possible output for the test that was set up. The second output had no new information in these tests and as seen in the table, the data entered were just zero. In test 11, the outputs Q_3 and RAM_3 shifted from a high impedance state to a zero state. Due to external circuits connected to RAM_3 and Q_3, the high impedance state appeared as a zero state and therefore no oscilloscope measurements were made for this test (value of 0.0 was entered in the table for test 11).

Although the MD-104 does not perform DC parametric tests, measurement of the sink and source currents for two of the most common output configurations (seen in Figure 4) were made during the dynamic test routine. The YO output and the Cn + 4 output was chosen as the representative for each output configuration. The output sink current (I_{OL}) was measured with an output voltage of 0.5 V. The source current (I_{OH}) was measured with an output voltage of 2.4 V. The total chip power consumption (I_{CC}) was also measured. All ot these tests were performed with the power supply voltage at 5.0 V and measurements were taken with a digital volt-ohmmeter. These data are presented at the bottom of the 26 dynamic tests (see Table 1).

Since the MD-104 is basically a pattern generator, an external circuit called a personality card had to be constructed to interface between the 2901A and the tester. This circuit contained instruction, address, and data latches; it insured that all the microprocessor timing constraints were met; and it also contained all the electronics for the dynamic test routines. A simplified diagram of the personality card is given in Figure 5. The MD-104 T-register (16 bits) contains the carry input, instruction word, and shift control inputs that are applied to the 2901A. Data for the 2901A direct inputs (DO-D3) come from either the MD-104 T-register or A-register depending upon control signals from the program. All addressing data for the A and B ports come from the Macrodata A-register. The A address port can be set equal to B address or to the inverse of B. The clock circuit allows regular clock pulses (5 MHz), clock inhibit (ZERO), or a constant ONE input on the clock line. All output data from the shift registers, status flags, and Y outputs are strobed into the MD-104 D-register. The dynamic tests are activated by pressing a switch which interrupts the functional tests. Light emitting diodes (LED) display the current

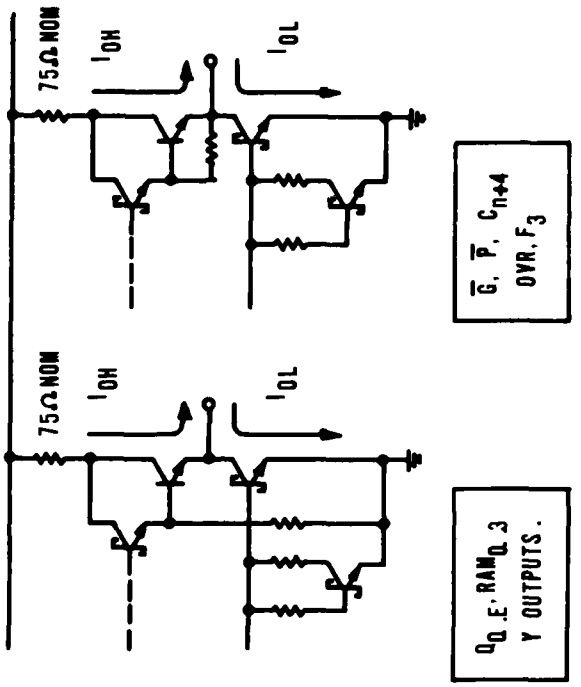


Figure 4. Output configuration of YO and Cn+4 used in measurements above.

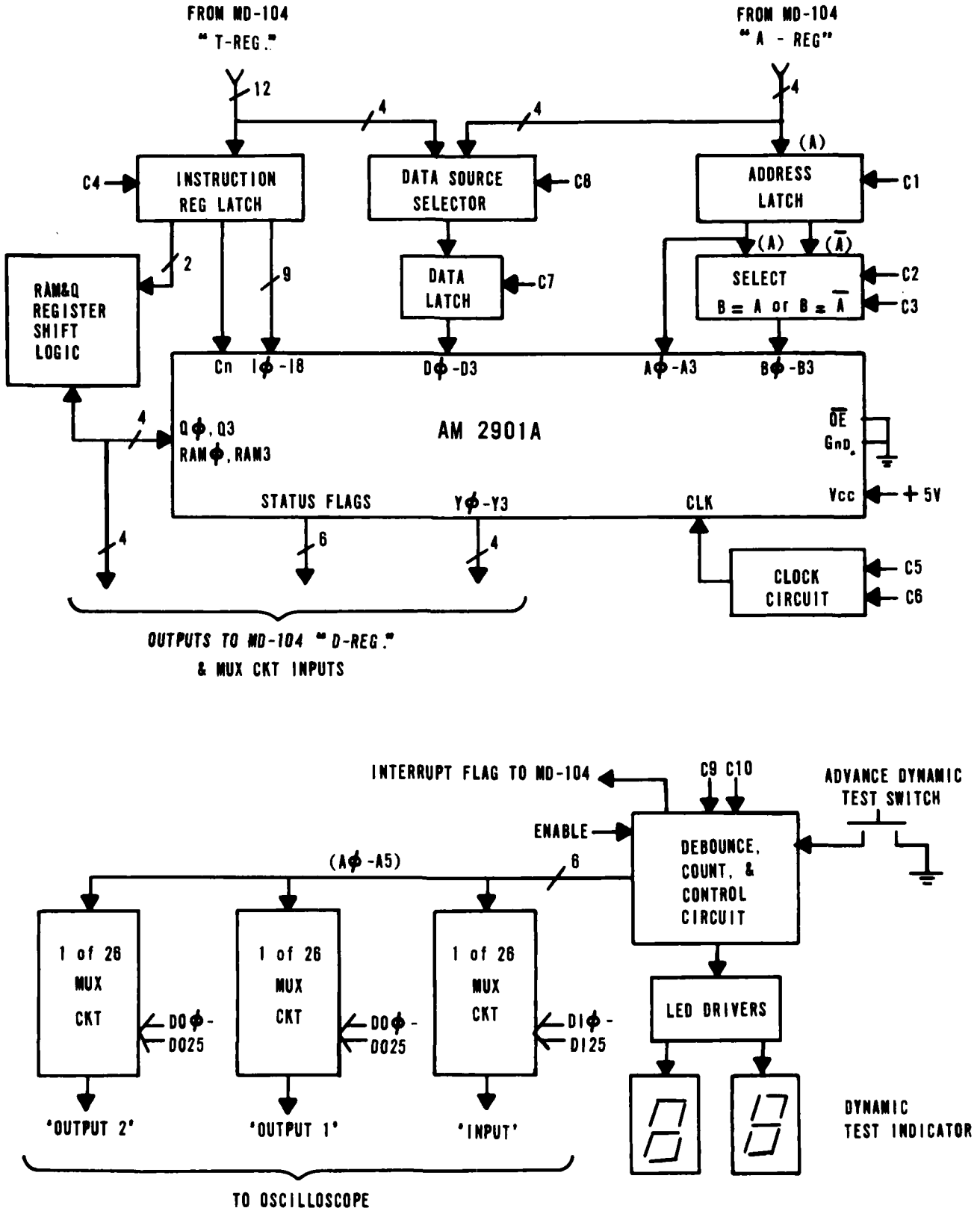


Figure 5. Block diagram of AM2901A interface board to MD-104

dynamic test number, and the multiplexer outputs contain the data for the propagation delay measurements.

The test program for the 2901A functions as follows. Upon completion of loading the program into the MD-104, and connecting the power supplies to the personality card which is inserted into the MD-104, the system is ready for functonal testing. The functional test can be looped until an error occurs, or run through a single time. If no error occurs, a green light indicates such. But if an error does occur, it is indicated by a red light; the MD-104 stops program execution and the Macrodata registers display the erroneous output of the 2901A, the expected output, the current instruction, the program step location, and other pertinent data useful for error analysis.

A sync pulse can be obtained on any program step. This is useful for triggering oscilloscopes and radiation sources on any desired test (described in more detail in dose-rate testing section). To start the dynamic tests, one simply presses a switch to obtain test 1. This sends out an interrupt flag to the functional program which, when acted upon, loops the first dynamic test. After switching through the 26 tests, it automatically cycles back to functional testing. The functional tests were designed such that even a threefold increase in propagation delay time would not cause a functional failure. Such degradation would be observed in the dynamic test routine.

Specific details on the MD-104 functional and dynamic tests are not presented in this report. To get a good understanding of the complete system operation would require a lengthy and complicated description of the interaction between the personality card, data buffer memory, and especially the software containing the algorithms for generating the patterns. Someone familiar with MD-104 operation and desiring further information on the 2901A program can contact Lt. Keith W. Loree, Air Force Weapons Laboratory (NTYCT), Kirtland AFB, NM 87117, Phone (505) 844-0316 or AUTOVON 244-0316.

III. RADIATION TEST RESULTS

The AM2901A was tested in neutron, total ionizing dose, and ionizing dose-rate environments. The devices were tested prior to irradiation and following each irradiation, using the functional and dynamic tests described in the previous section. All measurements and tests were conducted at room temperature (25°) with a power supply voltage $\left(V_{CC}\right)$ of 5.0 V.

NEUTRON TESTS

Ten 2901A microprocessors were tested at the Sandia Pulsed Reactor (SPR) facility. All neutron irradiations were performed passively with no bias applied to the devices. Given below are the desired fluences and the actual fluence received by each device as measured by sulfur dosimeters.

Test No.	Desired Fluence (n/cm^2)	Actual Fluence (n/cm^2 - 1 MeV equiv.)
1	1.0×10^{12}	1.1×10^{12}
2	5.0×10^{12}	6.0×10^{12}
3	1.0×10^{13}	1.1×10^{13}
4	4.0×10^{13}	3.6×10^{13}
5	7.0×10^{13}	- - - - -
6	1.0×10^{14}	1.1×10^{14}
7	4.0×10^{14}	4.2×10^{14}
8	7.0×10^{14}	7.4×10^{14}

A mix-up resulted in a fluence of 7.4×10^{13} n/cm^2 for shot 5 instead of 3.4×10^{13}. The total cumulative fluence for shot 5 was therefore 1.1×10^{14} $(3.6 + 7.4 \times 10^{13})$ instead of the desired 7×10^{13} n/cm^2. So no data exist at 7×10^{13} n/cm^2.

Pre- and post-irradiation tests consisted of functional and dynamic measurements using the MD-104 as described in Section II. Functionally and dynamically, all 10 microprocessors operated with specifications up to and including a total fluence of 1×10^{14} n/cm^2. However, by 4×10^{14} n/cm^2, 7 of 10 microprocessors failed the functional tests. The failures occurred during the RAM tests (test sets 1-6). Additional information about the failures was obtained from the propagation delay tests.

Tests 16-23 plus tests 25 and 26 (all involving use of the RAM register) showed errors for the devices that failed 4×10^{14} n/cm^2 (see Table 1 for description of tests). Test 16 for example, measures the propagation delay

between a change in the A port address (line A_0) and the Y outputs, bypassing the ALU. The RAM at address 6 ($A_3A_2A_1A_0$ = 0110) is written to ONEs, while the RAM at address 7 ($A_3A_2A_1A_0$ = 0111) is written to ZEROs. The address line A_0 is then alternated between 0 and 1, which in the read mode causes the output to to switch between 1 and 0. Figure 6 shows the results of test 16 at different power supply voltage levels V_{cc} for a failed device. As seen, at 5 V there was no output response for test 16 and test 17 (which uses different RAM locations and address lines for its test). Following is a comparison of the power supply voltage required to achieve the same propagation delay to a logic one $T_{pd}1$ as in the photographs for: (a) a nonirradiated device, (b) neutron device that survived 4 x 10^{14} n/cm^2, and (c) a neutron device that failed at 4 x 10^{14} n/cm^2.

$T_{pd}1$	Device (a)	Device (b)	Device (c)
(ns)	(V)	(V)	(V)
no pulse	3.58	4.75	5.56
380ns	3.62	4.86	5.74
180ns	3.72	5.00	5.88
50ns	4.25	5.50	6.30

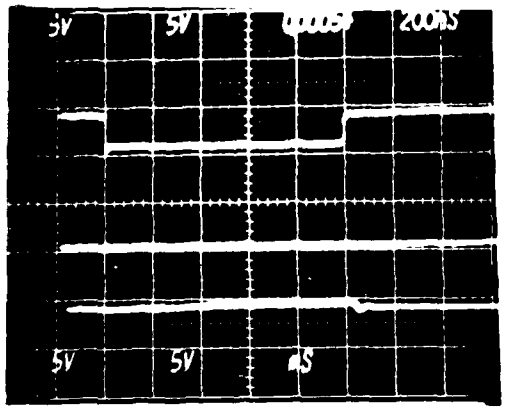
Oscilloscope traces for the above three devices looked identical, the only difference being the amount of biase required to produce the given delay. Note that the propagation delay to logic 0 $T_{pd}0$ remained constant throughout the tests.

For the remaining tests the devices failed had data outputs that went through the ALU. The large propagation delay increases observed in the previous tests were not seen, but for insufficient bias voltage, the outputs Y_3 - Y_0 oscillated. Figure 7 shows this for test 19, given a device that failed 4 x 10^{14} n/cm^2. Devices that failed, other than those in tests 16 and 17, had results vey similar to test 19. The voltage variation tests performed on a nonirradiated device again showed results identical to the neutron devices, only at much lower power supply voltages. At 6 V all failed devices passed the functional tests, and at 6.5 V the devices all had propagation delays equal to nonirradiated devices at 5 V.

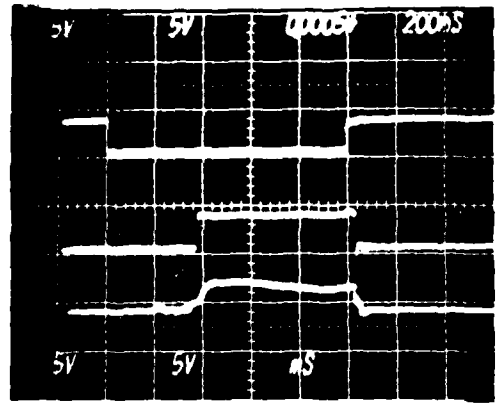
The three devices that were still functional at 5.0 V were then exposed to 7 x 10^{14} n/cm^2, and all three were still operational at 5.0 V. The average

Horizontal: 200 ns/div

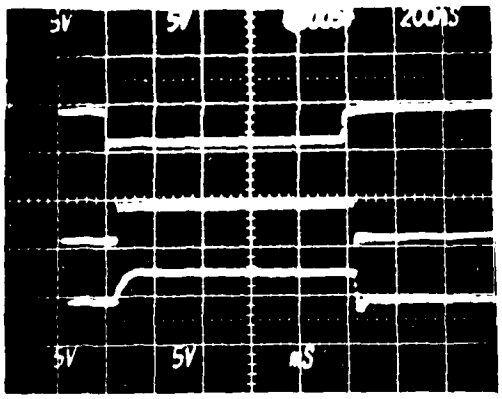
Vertical: 5 V/div



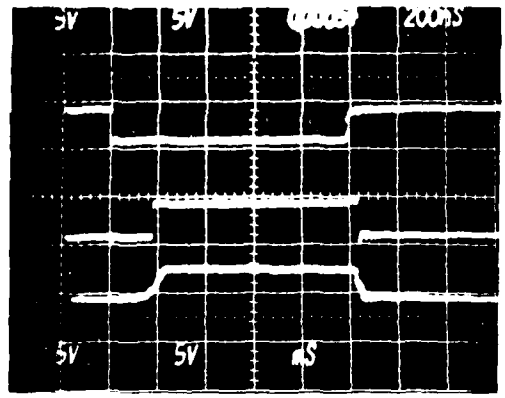
(a) V_{cc} 5.56 V; no output response



(b) V_{cc} = 5.74 V; $T_{pd}1$ = 380 ns



(c) V_{cc} = 5.88 V; $T_{pd}1$ = 180 ns

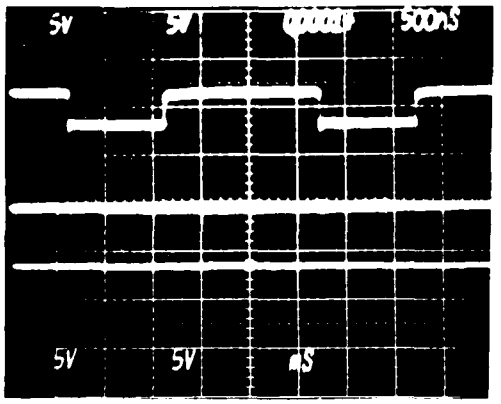


(d) V_{cc} = 6.3 V; $T_{pd}1$ = 50 ns

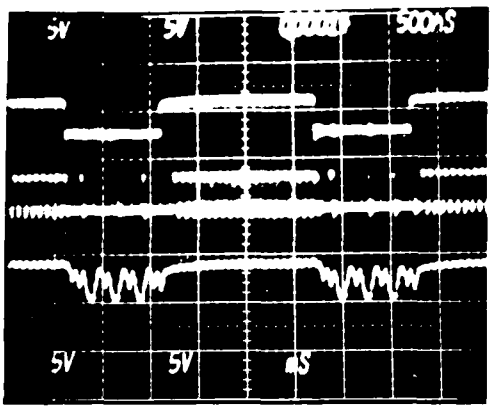
Figure 6. Test 16 propagation delay response for a failed device at various power supply (V_{cc}) levels. The top trace is the input (address line A_0). The bottom trace is the microprocessor output (Y_0), while the middle trace is that Y_0 output run through the dynamic test multiplexer circuit.

Horizontal: 500 ns/div

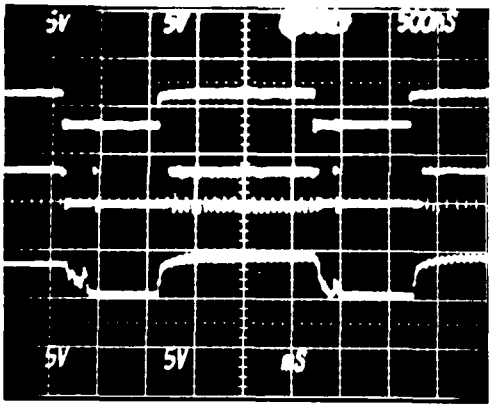
Vertical: 5 V/div



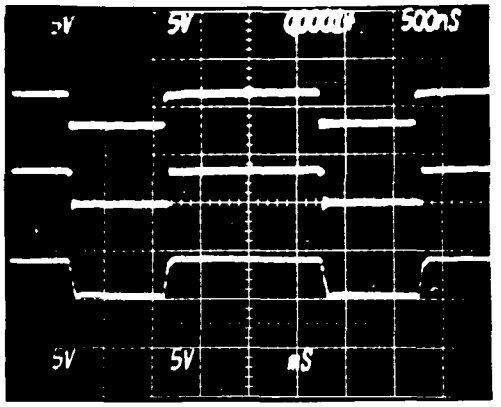
(a) V_{cc} = 5.00 V; no output response



(b) V_{cc} = 5.05 V; oscillating output



(c) V_{cc} = 5.20 V; oscillating output



(d) V_{cc} = 5.60 V; good output

Figure 7. Test 19 propagation delay response for a failed device at various power supply (V_{cc}) levels. The top trace is the input (address line A_0). The bottom trace is the microprocessor output (Y_2), while the middle trace is that Y_2 output run through the dynamic test multiplexer circuit.

of the 26 dynamic tests and parametric measurements for all functional devices at each radiation level are given in Appendix A. Table 2 shows the percent degradation from the preirradiation data for each of 26 propagation delay tests and current measurements (for functional devices only) at the various radiation levels. As seen in Table 2, even for the functional devices, the propagation delay and output sink/source currents start increasing substantially after 1×10^{14} n/cm^2. Only the functional devices are in the tables because failed devices often had no output response, or had an oscillating output at 5 V for which no measurements could be made. It is clear that the faulty output stems from RAM register circuitry degradation, since the output gates and status flags functioned properly in the remaining tests (even in the failed devices).

TOTAL DOSE TESTS

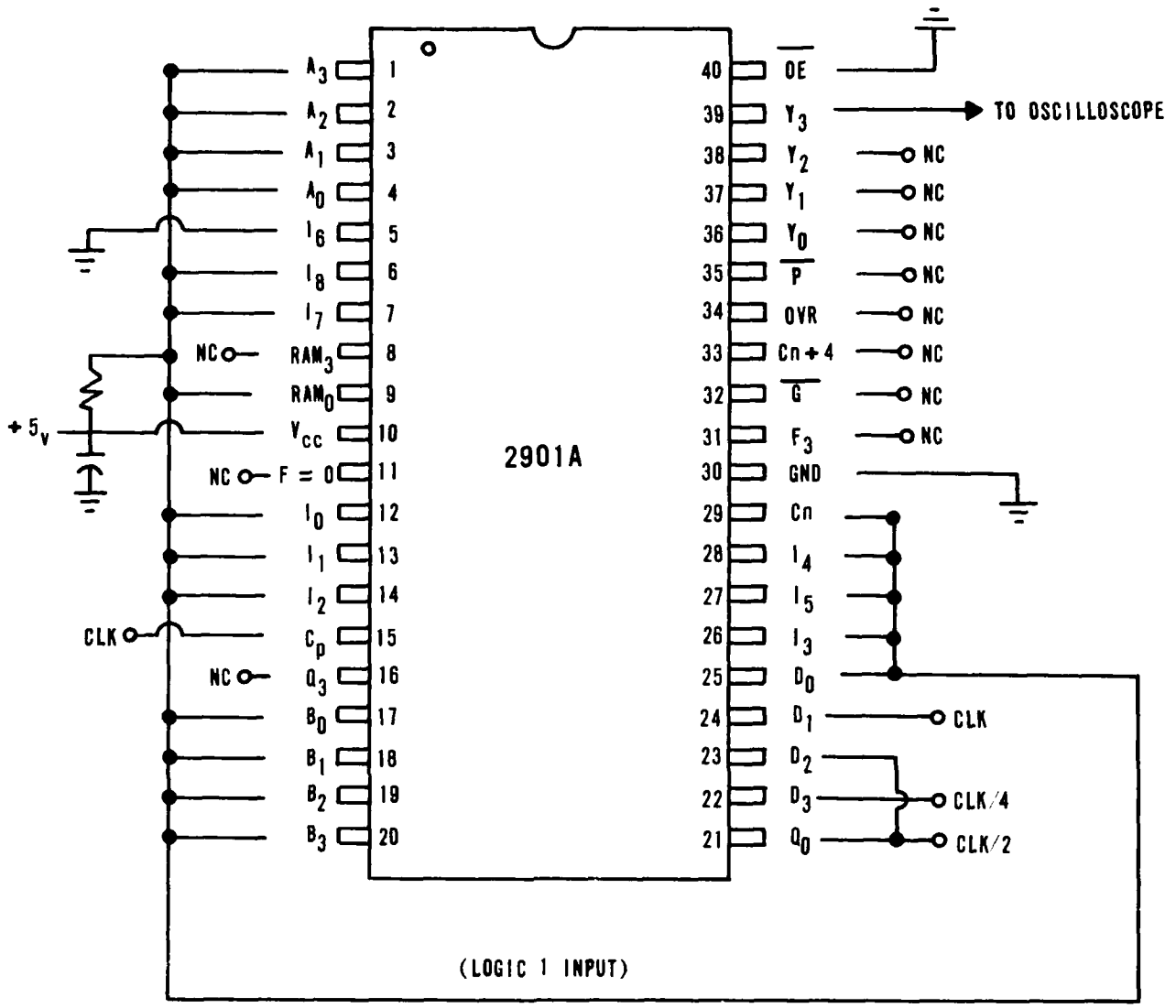
Total ionizing dose tests were performed on six AM2901A microprocessors. Full functional and dynamic measurements were made at the following cumulative total dose levels.

50 krads (Si)
100 krads (Si)
200 krads (Si)
300 krads (Si)
500 krads (Si)
700 krads (Si)
1 Mrad (Si)
3 Mrads (Si)
6 Mrads (Si)
9 Mrads (Si)

Tests through 1 Mrad total dose were performed at AFWL's gamma source. The larger dose levels were done at Sandia's Gamma Irradiation Facility (GIF), since it is a more active source requiring less time to reach the desired radiation level. Three microprocessors were unbiased during these tests, while the remaining three were cycled through repetitive right shift instructions I_{80} = 677 (performs both a RAM and Q shift). Pin connections for the actively biased devices are given in Figure 8. The clock (CLK) was a 4 MHz square wave with CLK/2 and CLK/4 simply obtained by running the clock through two J-k flip-flops. The only signal monitored during the irradiation was the Y_3 output which was identical to the CLK/4 signal.

TABLE 2. PERCENT CHANGE FROM PRE-IRRADIATION DATA FOLLOWING NEUTRON EXPOSURE

TEST NO.	1E+12	5E+12	1E+13	4E+13	1E+14	4E+14	7E+14
1	1.1	2.0	.8	-.4	1.4	7.5	30.1
2	1.4	3.4	2.5	1.6	4.6	14.1	39.5
3	2.4	3.6	3.6	2.2	8.8	18.4	46.4
4	.8	2.6	1.5	1.0	5.2	13.1	45.6
5	3.1	3.2	3.7	2.9	6.2	14.3	45.6
6	1.0	2.6	2.8	2.2	7.2	15.8	45.4
7	4.3	2.0	.4	-2.6	.0	7.1	29.1
8	.8	2.8	4.4	.6	5.4	16.0	45.4
9	.8	2.6	3.2	.6	1.6	13.4	45.6
10	1.0	3.1	2.1	2.0	8.2	12.7	48.6
11	.0	.0	.0	.0	.0	.0	.0
12	3.5	2.4	1.1	-1.9	-1.2	7.2	12.2
13	1.5	2.8	3.8	3.0	3.0	9.1	29.2
14	1.3	4.3	4.7	.9	-1.0	1.8	20.2
15	2.2	1.7	2.9	2.9	5.6	12.4	45.1
16	2.0	3.2	-2.4	1.9	5.6	9.5	42.6
17	.6	2.9	-1.8	2.0	6.5	10.1	51.8
18	2.7	4.2	1.5	1.6	2.6	8.7	31.5
19	.6	1.1	-.1	.2	-.5	3.3	33.5
20	2.3	3.5	1.9	2.6	8.1	11.1	37.2
21	1.4	1.1	1.5	.4	3.7	10.0	46.5
22	.0	2.0	2.6	2.5	3.0	13.2	20.4
23	-1.4	2.7	1.7	2.0	6.6	18.2	65.3
24	.7	3.2	.2	3.9	1.9	5.2	24.6
25	2.0	1.8	1.2	-.2	-.2	5.0	26.8
26	3.4	3.6	2.6	1.0	.6	3.6	16.8
AVERAGE PROPAGATION							
CHANGE:	1.7	2.7	2.2	1.9	3.9	10.4	37.0
POWER (Icc)	-.5	-.7	-.8	-2.3	-3.9	-16.7	-45.5
YO I(OL)	-.4	-1.8	-2.6	-6.9	-20.7	-48.1	-101.4
YO I(OH)	-.5	-1.8	-2.8	-7.8	-21.4	-62.5	-172.8
On+4 I(OL)	-.8	-1.3	-.8	-2.1	-7.7	-16.7	-24.0
On+4 I(OH)	-.4	-.9	-.9	-1.3	-15.8	-12.9	-26.1



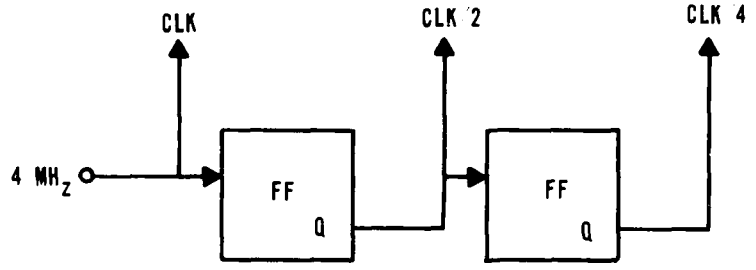


Figure 8. Pin connections for the actively biased devices.

All six devices were irradiated to the levels specified earlier until a functional failure occurred as determined by th MD-104 tester. At this point, only the remaining good devices were further irradiated. The only functional failures to occur were observed in the active devices. At 6 Mrads, two of the three microprocessors performing the right shift instructions failed the RAM tests (test sets 1-6). The remaining four devices were then tested to 9 Mrads to see if any additional failurs would result. All four devices still performed satisfactorily afterwards, which then concluded the radiation exposures.

Further examination of the errors in the actively irradiated devices showed some interesting results. Again using the 26 dynamic tests, it was observed that the same error conditions that occurred in the neutron devices also occurred in the actively biased total dose irradiated devices. Details on the error condition were given in the section on neutron tests.

Table 3 shows a summary of the percentage degradation from the preirradiation values for the 26 propagation tests, power supply current and output sink/source current at the given total dose levels (for functional devices only). Except for the two devices that failed, there were only minor increases in propagation delay throughout the range of the total dose radiation tests. Presented in Appendix B is the average of the above mentioned tests for the functional devices at each radiation level.

TRANSIENT RADIATION TESTS

Gamma dose-rate tests were performed on five AM2901A microprocessors to determine minimal logic upset levels, possible latch-up, and survivability. All tests were conducted at the Air Force Weapons Laboratory using the Febetron 705 Flash X-ray machine. The machine produces a 2 MeV burst wth a half-power pulse width of 20 ns. Larger dose-rates for device survivability were obtained using the FXR in a 2 MeV electron-beam mode of operation with a 50 ns pulse window.

Transient dose-rate testing required a remote test fixture for functionally exercising the device under test during irradiation. In order to retain sharp pulses at the 5 MHz clock speed, 38 line drivers (24 to the device and 14 to the return lines) were used to drive 30-ft lenghts of RG-58 50 Ω coaxial cable. Other than increases in propagation delay due to the cable and drivers, the microprocessor operated functionally as well in the remote fixture as on the personality board. Figure 9 presents a block diagram of the transient radiation test

TABLE 3. PERCENT CHANGE FROM PRE-IRRADIATION DATA FOLLOWING CO-60 EXPOSURE

TEST NO.	100K	300K	500K	700K	1MRAD	3MRAD	6MRAD	9MRAD
1	.5	3.3	3.3	3.2	4.7	3.7	5.1	11.1
2	1.4	7.2	4.5	1.5	4.4	2.1	5.5	8.4
3	1.2	5.2	4.4	2.8	6.2	9.8	8.2	11.6
4	-.2	5.1	3.4	3.2	5.4	6.3	7.2	9.7
5	.0	5.7	3.7	1.4	5.3	6.8	7.3	11.2
6	.6	3.4	2.8	1.2	4.4	6.2	5.4	6.2
7	.0	4.9	3.5	.8	3.6	1.4	6.4	8.2
8	.4	4.6	2.2	-.2	3.2	7.8	6.4	8.8
9	-.2	3.6	1.0	-1.8	1.8	5.8	7.0	9.6
10	-.6	4.3	3.7	3.8	8.3	8.0	8.9	13.6
11	.0	.0	.0	.0	.0	.0	.0	.0
12	1.2	3.1	-1.7	-3.9	-1.6	-4.7	-2.0	2.0
13	2.8	6.6	.8	1.2	3.1	3.6	3.3	6.6
14	2.1	4.8	3.5	-.7	3.1	5.8	6.4	10.2
15	1.7	3.8	2.7	-.1	3.0	5.8	6.6	8.2
16	2.1	6.9	4.2	4.2	10.3	7.6	7.8	11.5
17	-.8	4.0	2.5	1.2	7.0	8.3	6.4	10.8
18	3.2	7.6	6.7	7.5	10.8	12.2	11.2	22.6
19	-2.3	-.4	-4.2	-5.0	-1.9	-2.4	-3.7	5.3
20	1.1	4.5	4.0	3.6	7.8	9.4	9.9	14.9
21	-.7	3.3	3.2	3.0	4.3	6.3	7.6	13.7
22	-1.0	3.2	.2	-1.0	.0	-.2	1.0	6.8
23	-.8	4.4	1.8	1.4	5.6	5.9	6.8	10.7
24	-.3	3.4	1.4	.8	5.3	5.7	5.2	10.3
25	1.2	2.6	2.8	1.4	4.0	6.6	6.0	12.2
26	1.4	2.8	2.4	2.6	4.6	4.6	3.6	6.6
AVERAGE PROPAGATION CHANGE:	1.1	4.3	3.0	2.4	4.8	5.9	6.2	10.0
POWER (Icc)	-.1	-3.3	-4.2	-6.1	-4.5	-13.2	-8.0	-16.6
YO I(OL)	-2.2	-2.6	-1.8	-2.6	-7.7	-4.9	-21.3	-15.3
YO I(OH)	-2.3	-2.8	-2.0	-1.8	-7.2	-.9	-13.5	-10.9
Cn+4 I(OL)	.9	-1.4	-1.4	-1.0	-.5	-.9	-3.3	-2.8
Cn+4 I(OH)	-.5	-1.0	-1.0	-1.5	-2.5	-1.5	-7.8	-5.1

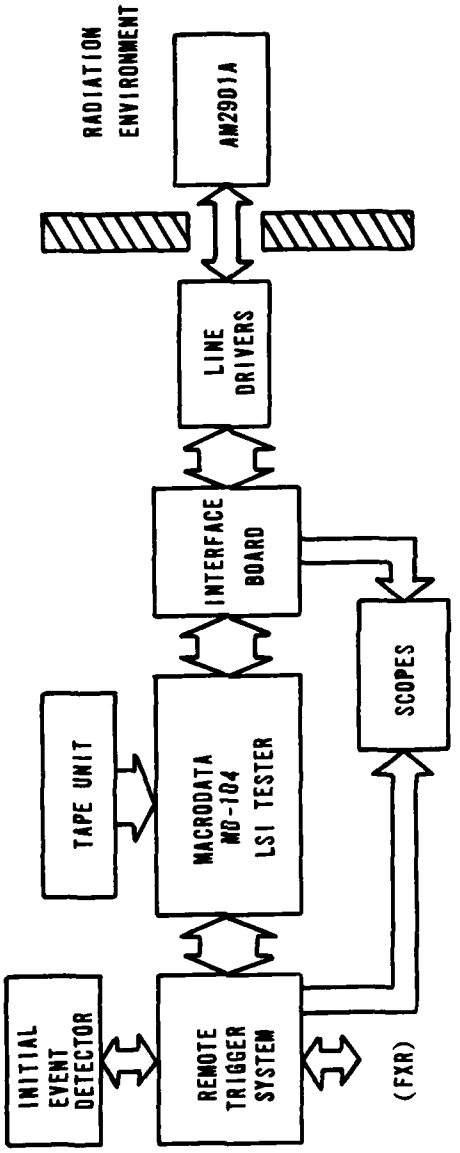


Figure 9. Block diagram of transient radiation test configuration.

set-up. Figure 10 is a photograph showing the Macrodata MD-104 tester with the AM2901A personality board connected and the line drivers going to the device under test (DUT). The photograph in Figure 11 is of the remote test box with the small printed circuit board on top holding the DUT. The line drivers sending the output signals back to the MD-104 are all shielded with lead bricks (partially removed for the picture). The test device receives its exposure through a 2-cm-diameter hole in the lead brick in front of the device.

To be able to position the FXR pulse at any predetermined point within the test program, the following procedure is used. The FXR console trigger pulse is used to start the MD-104 via an external trigger input. The MD-104 puts out a sync pulse whenever the program step and Macrodata A-register match that as preprogrammed by the operator. After some modification, this sync pulse is then used as the FXR trigger pulse. Since many algorithms are repeated during one full cycle of the functional test, multiple sync pulses are very likely to occur during the test. An initial event detector circuit is used to eliminate these undesired subsequent sync pulses. Besides the console trigger pulse, the remote triggering system consists of a Textronix 7D11 oscilloscope delay plug-in, a pulse shaper circuit, and a battery circuit which actually fires the machine. The single sync pulse run through a Textronix plug-in is used for fine positioning of the FXR pulse. This pulse is then lengthened to 1 μs, brought up to TTL levels, and used to fire the battery. Since the delay through the circuitry following the MD-104 sync pulse until the FXR fires is approximately 1000 ns, the sync pulse is programmed to occur 5 clock cycles earlier than the desired event (5 cycles at 5 MHz = 1000 ns). This procedure then allows testing of any desired instruction, input data, or output state.

The FXR tests were conducted during the RAM register, Q register, shift, and arithmetic operations, as well as during source and function OP code instruction checks, to determine which condition resulted in the minimum transient upset level. Minimum upset during the RAM register tests was 2.1×10^8 rads(Si)/s. Q register upset occurred at 5.0×10^8 rads(Si)/s. Determining upset levels of the shift operations, arithmetic operations, and several other functions was difficult since these tests all used data from the RAM registers. Upset levels on these operations occurred at dose rates equal to or greater than that of the RAM register tests. Where the dose rate upset level was the same, it was generally the RAM register which caused the error. From the dose rate testing conducted, it was evident that the RAM register was the first area of the AM2901A

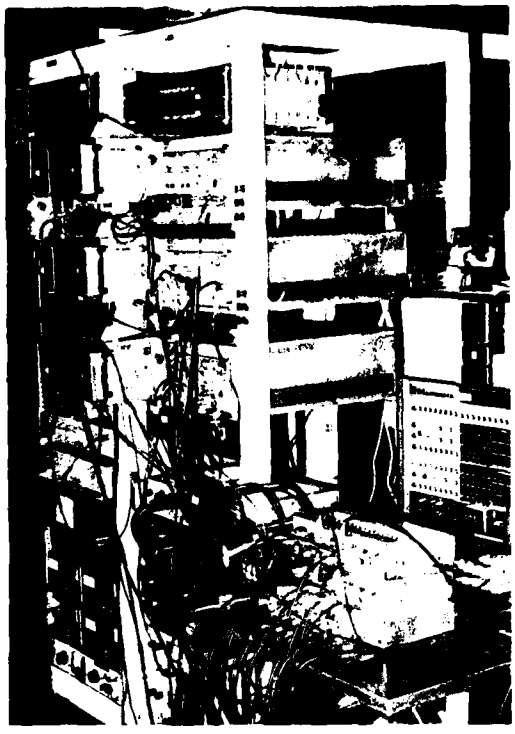


Figure 10. FXR test setup including MD-104, personality board, line drivers, and oscilloscopes.

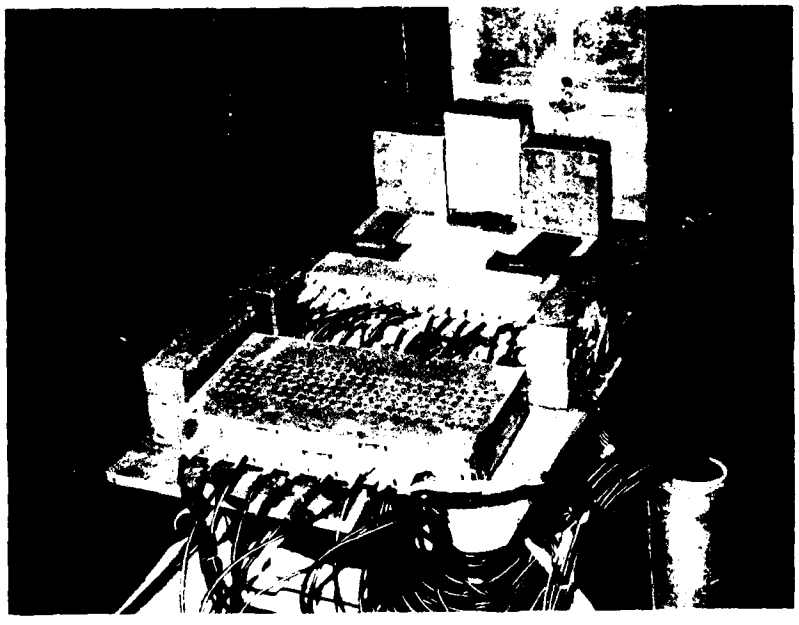


Figure 11. FXR remote 2901A test box in the shielded screen room with extra shielding around the line drivers and test box.

to experience transient upset.

RAM register testing consisted of checking five devices in the six RAM GALPAT tests (described in Section II) during the following operations:

(a) Rewriting the old odd bit to a background bit

(b) Writing the next background bit to the odd bit

(c) Reading the odd bit

(d) Reading various background bits

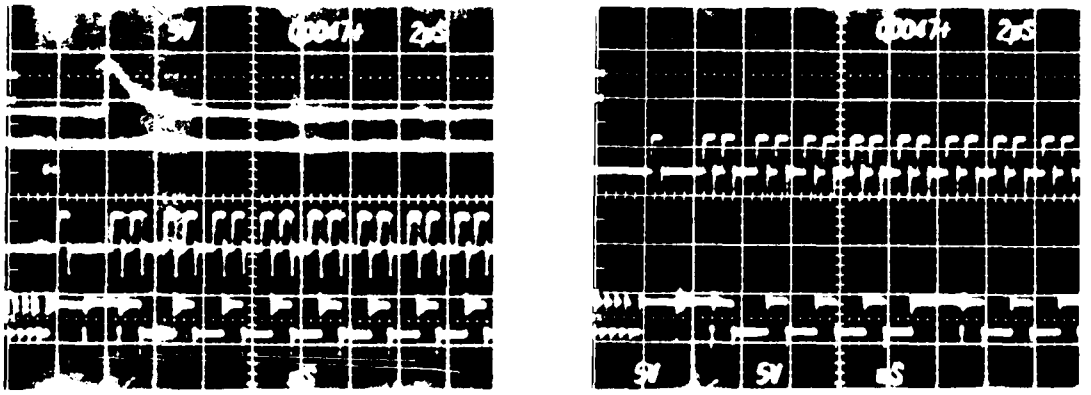
(e) During capture of RAM output data into the MD-104 data register

The resulting logic upsets were not what was expected. One would normally expect that the event occurring at the time of the FXR pulse would be distorted and therefore possibly be misinterpreted as a ZERO instead of a ONE or vice-versa. Instead, the earliest sign of FXR upset was that bits of information stored in the 16 x 4 two-port RAM were altered from a ZERO to ONE state. The bits remained in a ONE state during successive reads until the bits were rewritten in subsequent tests. Test sets 1-3 failed at slightly lower dose rates (2.1×10^8 rads(Si)/s than tests 4-6 (2.8×10^8 rads(Si)/s). Tests 1-3 failures occurred where the ZERO background bits turn to ONEs, while test 4-6 had failures where the single ZERO odd bit changed to ONE. Tests 1-3 probably failed at slightly lower levels than test sets 4-6 because of the larger percentage of ZEROs which could be altered to a ONE. No appreciable difference in upset levels occurred when positioning the FXR pulse at the five conditions stated above or when using different test devices. The FXR caused random alterations of bits from a ZERO to ONE state, independent of where and when the pulse occurred; an error would occur when checking the RAM locations for given data.

A typical test case is presented in which RAM test 3 (GALPAT pattern using the A port address and bypassing the ALU) was being checked. The FXR pulse occurred during the rewrite of the first odd bit (at address 0) to a background bit (ZERO state). The following memory locations were altered from the correct output of 0000 at a dose rate of 2.2×10^8 rads(Si)/s (there are four output bits at each memory location-- 16 x 4 memory).

$ADDR(A_3A_2A_1A_0)$	0011	0100	0110	1000	1001	1011	1100
$OUT\ (Y_3Y_2Y_1Y_0)$	0001	0010	0001	0001	0001	0011	1001
errors	↑	↑	↑	↑	↑	↑↑	↑ ↑

Shown below are some oscilloscope traces of the RAM register errors observed. Figure 12a is a preirradiation photograph of RAM register test set 1. The top trace is the FXR trigger pulse. The shot actually occurs 600 ns after the rising edge of this pulse. To prevent any upsets during this test, the FXR trigger was not connected to the machine. The second trace from the top displays the clock. The first clock pulse is needed to rewrite the old RAM odd bit to a ZERO, and the second clock pulse is used to write the odd bit (ONE) in the now incremented address. The third trace is the data strobe input (DSI) pulse which clocks data into the MD-104 for comparison (on the negative edge of the DSI). The GALPAT test starts with the successive DSI pulses after the single pulse. The first of these pulses latches the background data at address 0; the next DSI latches odd bit data at address 1 into the MD-104; the third DSI checks the background bit at address 2; the fourth again checks the odd bit at address 1, then 3, 1, 4, 1, 5, 1, etc. The bottom trace shows the output line (Y_0) that is latched into the MD-104 by the DSI pulses. Since the FXR pulse occurs 600 ns after the FXR trigger fires, it can be seen that the FXR shot occurs during the first GALPAT DSI pulse (reading the odd bit). The next photograph (Figure 12b) shows the same test shot as in Figure 12a, but with the FXR machine active. The dose-rate at the device under test was 2.1×10^8 rads(Si)/s. Displayed are the DSI pulses (top) and the output data (line Y_0). The background bit at address 6 was changed from a ZERO to ONE for this test. This was the only upset recorded on any of the four output lines for this shot.



(a) Preirradiation data during test

(b) Posttest results; DSI (top) upset output (bottom)

Figure 12. RAM test set No. 1

The photographs in Figure 13 are also posttest responses of RAM test set 3 at a dose-rate of 2.2×10^8 rads/s. Output Y_0 had two consecutive background bits altered to a ONE at address X and X + 1, while the Y_1 and Y_2 outputs were correct. Then at address X + 2, the Y_1 output data was incorrect while the other two data lines were good. The FXR burst occurred just prior to the start of the traces.

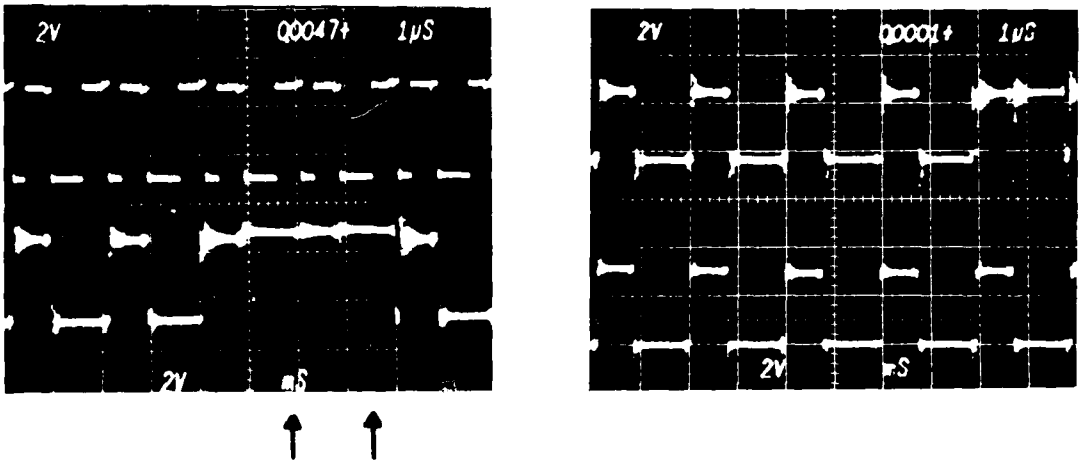


Figure 13. RAM register data altered from logic ONE to logic ZERO.

Three of the five AM2901A microprocessors were also tested for possible latch-up or burnout at the maximum X-ray dose-rate obtainable (5×10^{10} rads(Si)/s). Shots were conducted during RAM register, Q register, shift, and arithmetic operations. All devices experienced functional errors; however, all devices were completely operational following reinitialization of the test program. No changes in power supply current levels were noticed after the bursts.

The remaining two devices were also tested for survivability in the electron-beam mode of operation of the FXR machine. The devices were tested in a vacuum chamber test cell, the AM2901A's were exercised in a fixed mode with the RAM shift instructions continuously applied, just as in the total dose tests. Again, no sign of latch-up was observed as the power supply current remained unchanged after the FXR burst. The device was then removed from the test chamber and reevaluated using the MD-104 function and dynamic test routines. Both devices operated satisfactorily after the electron beam tests. There were only two electron beam test shots performed on each device, since a substantial total dose (2×10^{12} rads(Si)/s x 50 ns = 100 krads) was accumulated with each exposure and no deleterious responses were observed.

IV. CONCLUSIONS

Using the vendor developed test sets, breaking them into algorithmic patterns, and programming a Macrodata MD-104 wth these patterns proved to be an effective testing approach in the radiation evaluation of the AM2901A microprocessor. Being able to obtain and use the vendor's input and output test patterns resulted in a substantial reduction of several man-months of effort by not having to develop a test set to verify operation of the DUT. Since the intent of the project was to perform a radiation evaluation, and not a full electrical characterization of the 2901A, further investigation into the vendors test set to assure complete coverage of all the internal logic gates was not performed. The main drawback of the algorithmic pattern generation technique was the large amount of time required to set up the whole experiment. Developing the algorithmic patterns from the vendor information, designing the personality card between the 2901A and the MD-104 tester, and then troubleshooting the software and hardware required approximately 1 man-year. This was an initial attempt using this procedure, subsequent microprocessors evaluations with the same complexity vendor test sets could probably be set up in 7 to 9 man-months because of the experience gained from these tests.

The radiation tolerance of the low-power Schottky, bit-slice AM2901A was good, considering it is an unhardened commercially available LSI microprocessor. No failures were observed due to Co-60 total gamma dose irradiation through 3 Mrads(Si). Six devices were tested, of which 3 were actively biased (executing continuous shift instructions). Two of these biased devices failed between 3 and 6 Mrads(Si). No failures were observed on the unbiased devices through 9 Mrads(Si). Of 10 devices tested in a neutron environment, no failures were observed until between a fluence of 1×10^{14} and 4×10^{14} n/cm^2, where 7 of the microprocessors failed the functonal tests. Diagnosis of the errors using the functional and dynamic routines revealed that all device failures in both environments resulted from the same problem. The increase in access time (from 40 ns to over 250 ns) between changes in the RAM address and the output caused the functional errors. In transient ionizing dose-rate testing, logic upset occurred at 2.1×10^8 rads(Si)/s. Minimum upset resulted from ZERO states in the 16 x 4 RAM being altered to ONE states. All devices were fully operational after test program reinitialization. No latch-up, burnout, or hard failures were observed with tests up to 2×10^{12} rads(Si)/s using the FXR in the electron beam mode.

As seen by the AM2901A tests, functional evaluation using the MD-104 tester with modular test techniques worked well to detect faults. The earliest detectable radiation induced faults for the AM2901A all involved the 16 x 4 RAM registers during the dose-rate, neutron, and total dose environments. Potential hardening work conducted on the AM2901A should include improvements in the memory array and it's associated peripheral circuit design.

APPENDIX A
DYNAMIC TEST DATA FOR NEUTRON IRRADIATED DEVICES

AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: NEUTRON PRE-RAD NO. OF DEVICES: 10

TEST NO.	INPUT	OUT1 (ns):	tPd0	tPd1	OUT2 (ns):	tPd0	tPd1
1	D0	Y0	33.1	30.4	Y3	33.3	33.6
2	D3	G'	20.9	18.9	OVR	32.8	32.5
3	Cn	RAM0	42.7	29.2	RAM0	.0	.0
4	I0	Y1	33.3	30.8	F3	39.1	27.5
5	I0	G'	20.1	28.0	OVR	47.3	35.1
6	D0	RAM0	44.5	35.0	RAM0	.0	.0
7	I5	Y0	26.6	17.7	Y2	21.4	13.2
8	I5	RAM0	42.4	23.1	RAM0	.0	.0
9	I5	Cn+4	33.4	33.2	Cn+4	.0	.0
10	I4	F=0	35.4	66.0	F3	37.6	24.8
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	18.7	16.2	RAM3	16.2	16.2
13	CLK	Q0	15.2	28.8	RAM0	46.2	55.3
14	CLK	Y0	32.6	37.6	Y0	32.6	37.6
15	CLK	Cn+4	44.2	54.3	Cn+4	44.3	54.3
16	A0	Y0	25.5	32.4	Y2	19.7	27.2
17	A3	Y1	21.0	28.7	Y3	20.6	28.7
18	B0	Y0	57.5	45.7	P'	51.0	30.8
19	A0	Y2	43.3	47.1	Cn+4	45.7	49.8
20	B2	G'	45.6	35.7	OVR	52.4	54.6
21	A2	G'	43.6	29.3	OVR	46.0	51.4
22	Cn	OVR	21.2	17.6	OVR	.0	.0
23	Cn	Y0	29.0	24.3	Cn+4	22.7	17.0
24	I8	Y3	22.1	23.3	Y1	19.3	23.6
25	CLK	Y1	51.3	.0	F=0	.0	63.1
26	CLK	Y3	.0	51.2	F3	.0	52.3

POWER SUPPLY CURRENT (I_{CC}) = 131.5 mA

OUTPUT SINK CURRENT: Y0 I_{OL} = 28.0 mA Cn+4 I_{OL} = 23.6 mA

OUTPUT SOURCE CURRENT: Y0 I_{OH} = 22.1 mA Cn+4 I_{OH} = 22.7 mA

AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: NEUTRON - 1 x 10E+12 N/CM**2 NO. OF DEVICES: 10

TEST NO.	INPUT	OUT1 (ns):	tPd0	tPd1	OUT2 (ns):	tPd0	tPd1
1	D0	Y0	33.1	31.2	Y3	33.3	34.2
2	D3	G'	21.0	19.2	OVR	34.1	32.4
3	Cn	RAM0	43.5	30.1	RAM0	.0	.0
4	I0	Y1	33.5	31.4	F3	39.1	27.7
5	I0	G'	20.1	29.6	OVR	47.8	37.1
6	D0	RAM0	45.2	35.2	RAM0	.0	.0
7	I5	Y0	26.7	19.4	Y2	21.0	14.4
8	I5	RAM0	42.6	23.4	RAM0	.0	.0
9	I5	Cn+4	33.7	33.4	Cn+4	.0	.0
10	I4	F=0	36.0	66.7	F3	38.0	24.8
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	19.7	16.5	RAM3	17.0	16.5
13	CLK	Q0	15.0	29.1	RAM0	48.3	56.2
14	CLK	Y0	33.2	37.9	Y0	33.2	37.9
15	CLK	Cn+4	45.4	55.3	Cn+4	45.4	55.3
16	A0	Y0	25.5	33.5	Y2	19.6	28.6
17	A3	Y1	20.9	29.5	Y3	20.1	29.4
18	B0	Y0	59.3	47.0	P'	52.7	31.3
19	A0	Y2	42.6	48.1	Cn+4	45.7	50.7
20	B2	G'	46.5	36.7	OVR	53.4	55.9
21	A2	G'	43.2	31.1	OVR	46.3	51.3
22	Cn	OVR	21.9	17.0	OVR	.0	.0
23	Cn	Y0	28.6	24.7	Cn+4	23.7	15.7
24	I8	Y3	22.0	24.1	Y1	18.8	24.2
25	CLK	Y1	52.5	.0	F=0	.0	84.5
26	CLK	Y3	.0	52.9	F3	.0	54.1

POWER SUPPLY CURRENT (Icc) = 130.9 mA

OUTPUT SINK CURRENT :	Y0	I(OL) =	27.9 mA	Cn+4	I(OL) =	23.6 mA
OUTPUT SOURCE CURRENT:	Y0	I(OH) =	22.0 mA	Cn+4	I(OH) =	22.6 mA

AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: NEUTRON - 5 x 10E+12 N/CM**2 NO. OF DEVICES: 10

TEST NO.	INPUT	OUT1 (ns):	tpd0	tpd1	OUT2 (ns):	tpd0	tpd1
1	D0	Y0	33.9	31.0	Y3	34.1	34.0
2	D3	G'	21.6	19.6	OVR	34.6	32.8
3	Cn	RAM0	44.2	30.3	RAM0	.0	.0
4	I0	Y1	34.2	31.7	F3	40.2	28.0
5	I0	G'	20.5	29.6	OVR	47.6	36.6
6	D0	RAM0	45.5	36.2	RAM0	.0	.0
7	I5	Y0	27.2	18.3	Y2	21.9	13.2
8	I5	RAM0	43.7	23.7	RAM0	.0	.0
9	I5	Cn+4	34.2	34.1	Cn+4	.0	.0
10	I4	F=0	36.6	67.0	F3	38.6	26.0
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	18.8	17.0	RAM3	16.1	17.0
13	CLK	Q0	15.7	29.5	RAM0	48.2	55.9
14	CLK	Y0	33.5	39.8	Y0	33.5	39.8
15	CLK	Cn+4	45.6	54.5	Cn+4	45.6	54.5
16	A0	Y0	25.9	32.4	Y2	20.5	29.1
17	A3	Y1	21.5	29.8	Y3	21.1	29.5
18	B0	Y0	58.4	48.3	P'	52.7	32.7
19	A0	Y2	44.1	48.2	Cn+4	46.1	49.4
20	B2	G'	47.2	37.3	OVR	54.0	56.2
21	A2	G'	43.8	30.4	OVR	46.4	51.0
22	Cn	OVR	21.9	17.7	OVR	.0	.0
23	Cn	Y0	30.2	26.1	Cn+4	23.5	16.7
24	I8	Y3	22.6	24.3	Y1	19.8	24.5
25	CLK	Y1	52.6	.0	F=0	.0	84.1
26	CLK	Y3	.0	53.1	F3	.0	54.1

POWER SUPPLY CURRENT (I_{CC}) = 130.6 mA

OUTPUT SINK CURRENT : Y0 I(OL) = 27.5 mA Cn+4 I(OL) = 23.5 mA
OUTPUT SOURCE CURRENT: Y0 I(OH) = 21.7 mA Cn+4 I(OH) = 22.5 mA

AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: NEUTRON - 1 x 10E+13 N/CM**2 NO. OF DEVICES: 10

TEST NO.	INPUT	OUT1 (ns):	tPd0	tPd1	OUT2 (ns):	tPd0	tPd1
1	D0	Y0	33.4	30.8	Y3	33.7	33.5
2	D3	G'	21.7	19.1	OVR	34.0	33.0
3	Cn	RAM0	44.1	30.4	RAM0	.0	.0
4	I0	Y1	34.0	31.1	F3	40.0	27.7
5	I0	G'	21.2	29.3	OVR	48.1	36.1
6	D0	RAM0	44.9	36.6	RAM0	.0	.0
7	I5	Y0	26.5	17.7	Y2	22.6	12.7
8	I5	RAM0	43.6	24.5	RAM0	.0	.0
9	I5	Cn+4	34.8	33.9	Cn+4	.0	.0
10	I4	F=0	36.6	66.5	F3	38.4	25.3
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	18.4	16.9	RAM3	15.8	16.9
13	CLK	Q0	16.1	29.5	RAM0	48.2	56.6
14	CLK	Y0	33.5	40.1	Y0	33.5	40.1
15	CLK	Cn+4	45.8	55.5	Cn+4	45.8	55.5
16	A0	Y0	25.6	30.0	Y2	20.3	25.7
17	A3	Y1	21.9	26.8	Y3	21.3	26.3
18	B0	Y0	57.8	46.7	P'	52.0	31.2
19	A0	Y2	42.4	47.4	Cn+4	45.9	50.2
20	B2	G'	46.8	36.7	OVR	52.2	55.9
21	A2	G'	43.3	31.0	OVR	46.3	51.6
22	Cn	OVR	22.1	17.8	OVR	.0	.0
23	Cn	Y0	30.0	24.7	Cn+4	23.5	17.1
24	I8	Y3	21.9	23.9	Y1	18.9	23.9
25	CLK	Y1	52.1	.0	F=0	.0	83.7
26	CLK	Y3	.0	52.8	F3	.0	53.3

POWER SUPPLY CURRENT (Icc) = 130.4 mA

OUTPUT SINK CURRENT :	Y0	I(OL) =	27.3 mA	Cn+4	I(OL) =	23.6 mA
OUTPUT SOURCE CURRENT:	Y0	I(OH) =	21.5 mA	Cn+4	I(OH) =	22.5 mA

AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: NEUTRON - 4 x 10E+13 N/CM**2 NO. OF DEVICES: 10

TEST NO.	INPUT	OUT1 (ns):	tPd0	tPd1	OUT2 (ns):	tPd0	tPd1
1	D0	Y0	33.0	30.0	Y3	33.6	33.3
2	D3	G'	21.5	18.7	OVR	34.4	32.4
3	Cn	RAM0	44.8	29.1	RAM0	.0	.0
4	I0	Y1	33.9	30.6	F3	40.5	27.3
5	I0	G'	21.6	29.1	OVR	48.3	34.5
6	D0	RAM0	45.5	35.7	RAM0	.0	.0
7	I5	Y0	26.4	17.0	Y2	21.6	12.3
8	I5	RAM0	43.5	22.8	RAM0	.0	.0
9	I5	Cn+4	34.0	33.0	Cn+4	.0	.0
10	I4	F=0	35.7	66.6	F3	38.6	25.7
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	18.0	16.4	RAM3	15.2	16.4
13	CLK	Q0	15.5	29.5	RAM0	48.2	57.2
14	CLK	Y0	33.0	37.8	Y0	33.0	37.8
15	CLK	Cn+4	45.4	56.0	Cn+4	45.4	56.0
16	A0	Y0	25.4	32.6	Y2	20.1	28.7
17	A3	Y1	21.1	29.6	Y3	21.0	29.4
18	B0	Y0	57.4	46.3	P'	52.9	31.3
19	A0	Y2	43.1	46.0	Cn+4	45.8	51.5
20	B2	G'	47.6	36.2	OVR	53.3	56.1
21	A2	G'	43.4	29.6	OVR	46.2	51.8
22	Cn	OVR	24.1	17.4	OVR	.0	.0
23	Cn	Y0	29.8	24.6	Cn+4	25.0	16.4
24	I8	Y3	24.2	23.7	Y1	20.1	23.7
25	CLK	Y1	51.8	.0	F=0	.0	82.1
26	CLK	Y3	.0	52.0	F3	.0	52.6

POWER SUPPLY CURRENT (Icc) = 128.5 mA

OUTPUT SINK CURRENT :	Y0	I(OL) =	26.2 mA	Cn+4	I(OL) =	23.3 mA
OUTPUT SOURCE CURRENT:	Y0	I(OH) =	20.5 mA	Cn+4	I(OH) =	22.4 mA

AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: NEUTRON - 1 x 10E+14 N/CM**2 NO. OF DEVICES: 10

TEST NO.	INPUT	OUT1 (ns):	tPd0	tPd1	OUT2 (ns):	tPd0	tPd1
1	D0	Y0	33.5	30.5	Y3	34.4	33.9
2	D3	G'	22.7	18.6	OVR	36.3	32.7
3	Cn	RAM0	48.1	30.7	RAM0	.0	.0
4	I0	Y1	34.8	31.8	F3	43.1	28.3
5	I0	G'	22.3	28.7	OVR	49.8	37.2
6	D0	RAM0	49.5	36.1	RAM0	.0	.0
7	I5	Y0	26.6	17.2	Y2	22.2	13.1
8	I5	RAM0	46.9	23.1	RAM0	.0	.0
9	I5	Cn+4	35.9	31.8	Cn+4	.0	.0
10	I4	F=0	39.6	67.4	F3	41.7	26.8
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	17.7	16.8	RAM3	15.1	16.8
13	CLK	Q0	14.2	30.9	RAM0	47.2	60.3
14	CLK	Y0	31.6	38.0	Y0	31.6	38.0
15	CLK	Cn+4	46.6	57.5	Cn+4	46.6	57.5
16	A0	Y0	24.9	35.0	Y2	20.1	31.2
17	A3	Y1	21.4	32.0	Y3	21.2	31.5
18	B0	Y0	60.1	45.5	P'	54.8	30.4
19	A0	Y2	41.6	44.4	Cn+4	47.6	51.5
20	B2	G'	53.0	36.2	OVR	55.1	53.9
21	A2	G'	46.8	28.5	OVR	47.5	54.9
22	Cn	OVR	23.1	17.1	OVR	.0	.0
23	Cn	Y0	30.1	25.2	Cn+4	28.9	16.0
24	I8	Y3	22.9	23.6	Y1	19.8	23.6
25	CLK	Y1	52.1	.0	F=0	.0	81.5
26	CLK	Y3	.0	51.9	F3	.0	52.3

POWER SUPPLY CURRENT (Icc) = 126.6 mA

OUTPUT SINK CURRENT : Y0 I(OL) = 23.2 mA Cn+4 I(OL) = 22.1 mA
OUTPUT SOURCE CURRENT: Y0 I(OH) = 18.2 mA Cn+4 I(OH) = 19.6 mA

AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: NEUTRON - 4 x 10E+14 N/CM**2 NO. OF DEVICES: 3

TEST NO.	INPUT	OUT1 (ns):	tPd0	tPd1	OUT2 (ns):	tPd0	tPd1
1	D0	Y0	36.3	31.0	Y3	38.0	35.0
2	D3	G'	25.7	20.0	OVR	40.3	34.0
3	Cn	RAM0	54.7	31.7	RAM0	.0	.0
4	I0	Y1	38.3	32.0	F3	48.7	30.0
5	I0	G'	25.0	30.3	OVR	54.0	38.7
6	D0	RAM0	56.0	37.0	RAM0	.0	.0
7	I5	Y0	29.0	17.7	Y2	24.7	13.7
8	I5	RAM0	53.7	24.3	RAM0	.0	.0
9	I5	Cn+4	43.3	32.3	Cn+4	.0	.0
10	I4	F=0	41.0	69.0	F3	45.7	27.0
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	18.0	19.3	RAM3	15.3	19.3
13	CLK	Q0	14.0	34.0	RAM0	49.3	66.0
14	CLK	Y0	31.7	40.0	Y0	31.7	40.0
15	CLK	Cn+4	48.7	62.3	Cn+4	48.7	62.3
16	A0	Y0	25.7	35.7	Y2	21.3	32.3
17	A3	Y1	22.7	32.0	Y3	22.7	31.7
18	B0	Y0	64.3	46.7	P'	61.3	31.0
19	A0	Y2	42.3	47.3	Cn+4	50.0	52.7
20	B2	G'	53.7	37.0	OVR	60.0	59.3
21	A2	G'	49.0	30.0	OVR	52.3	57.3
22	Cn	OVR	26.3	18.0	OVR	.0	.0
23	Cn	Y0	29.7	25.3	Cn+4	38.7	16.7
24	I8	Y3	24.3	23.7	Y1	21.0	23.7
25	CLK	Y1	55.3	.0	F=0	.0	85.0
26	CLK	Y3	.0	53.3	F3	.0	54.0

POWER SUPPLY CURRENT (Icc) = 112.7 mA

OUTPUT SINK CURRENT :	Y0	I(OL) =	18.9 mA	Cn+4	I(OL) =	20.4 mA
OUTPUT SOURCE CURRENT:	Y0	I(OH) =	13.6 mA	Cn+4	I(OH) =	20.1 mA

AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: NEUTRON - 7 x 10E+14 N/CM**2 NO. OF DEVICES: 1

TEST NO.	INPUT	OUT1 (ns):	tPd0	tPd1	OUT2 (ns):	tPd0	tPd1
1	D0	Y0	45.0	35.0	Y3	48.0	42.0
2	D3	G'	32.0	21.0	OVR	52.0	44.0
3	Cn	RAM0	71.0	37.0	RAM0	.0	.0
4	I0	Y1	47.0	38.0	F3	66.0	41.0
5	I0	G'	34.0	33.0	OVR	67.0	54.0
6	D0	RAM0	76.0	42.0	RAM0	.0	.0
7	I5	Y0	34.0	22.0	Y2	29.0	17.0
8	I5	RAM0	70.0	29.0	RAM0	.0	.0
9	I5	Cn+4	64.0	33.0	Cn+4	.0	.0
10	I4	F=0	55.0	93.0	F3	62.0	33.0
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	17.0	22.0	RAM3	14.0	22.0
13	CLK	Q0	14.0	43.0	RAM0	57.0	84.0
14	CLK	Y0	35.0	50.0	Y0	35.0	50.0
15	CLK	Cn+4	60.0	84.0	Cn+4	60.0	84.0
16	A0	Y0	30.0	57.0	Y2	27.0	38.0
17	A3	Y1	28.0	37.0	Y3	28.0	60.0
18	B0	Y0	77.0	52.0	P'	84.0	35.0
19	A0	Y2	48.0	52.0	Cn+4	87.0	61.0
20	B2	G'	66.0	42.0	OVR	78.0	75.0
21	A2	G'	74.0	32.0	OVR	67.0	83.0
22	Cn	OVR	27.0	20.0	OVR	.0	.0
23	Cn	Y0	42.0	28.0	Cn+4	65.0	20.0
24	I8	Y3	31.0	25.0	Y1	28.0	25.0
25	CLK	Y1	64.0	.0	F=0	.0	107.0
26	CLK	Y3	.0	59.0	F3	.0	62.0

POWER SUPPLY CURRENT (Icc) = 90.4 mA

OUTPUT SINK CURRENT :	Y0	I(OL) =	13.9 mA	Cn+4	I(OL) =	13.2 mA
OUTPUT SOURCE CURRENT:	Y0	I(OH) =	8.1 mA	Cn+4	I(OH) =	18.0 mA

APPENDIX B

DYNAMIC TEST DATA FOR TOTAL DOSE IRRADIATED DEVICES

AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: TOTAL DOSE - PRE RAD NO. OF DEVICES: 6

TEST NO.	INPUT	OUT1 (ns):	tPd0	tPd1	OUT2 (ns):	tPd0	tPd1
1	D0	Y0	32.3	30.3	Y3	31.5	32.5
2	D3	G'	19.5	18.8	OVR	31.8	31.3
3	Cn	RAM0	41.0	28.8	RAM0	.0	.0
4	I0	Y1	31.5	30.2	F3	36.7	26.2
5	I0	G'	18.3	27.7	OVR	45.5	35.7
6	D0	RAM0	42.5	34.5	RAM0	.0	.0
7	I5	Y0	25.3	18.2	Y2	20.2	12.8
8	I5	RAM0	40.3	22.5	RAM0	.0	.0
9	I5	Cn+4	30.8	32.5	Cn+4	.0	.0
10	I4	F=0	36.3	59.3	F3	35.8	23.7
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	18.0	16.0	RAM3	15.7	16.2
13	CLK	Q0	15.8	28.3	RAM0	46.5	53.8
14	CLK	Y0	33.0	36.8	Y0	32.8	37.0
15	CLK	Cn+4	43.5	52.8	Cn+4	43.7	52.8
16	A0	Y0	25.0	32.5	Y2	19.3	27.7
17	A3	Y1	20.0	28.7	Y3	20.0	28.2
18	B0	Y0	54.5	46.3	P'	50.0	30.7
19	A0	Y2	37.0	50.2	Cn+4	45.5	48.5
20	B2	G'	43.8	35.7	OVR	51.0	53.5
21	A2	G'	40.3	29.2	OVR	44.0	48.7
22	Cn	OVR	20.5	16.7	OVR	.0	.0
23	Cn	Y0	28.8	25.3	Cn+4	21.8	15.5
24	I8	Y3	20.5	23.0	Y1	17.2	23.5
25	CLK	Y1	49.3	.0	F=0	.0	78.0
26	CLK	Y3	.0	50.8	F3	.0	51.7

POWER SUPPLY CURRENT (Icc) = 135.4 mA

OUTPUT SINK CURRENT :	Y0	I(OL) =	28.5 mA	Cn+4	I(OL) =	22.8 mA
OUTPUT SOURCE CURRENT:	Y0	I(OH) =	22.7 mA	Cn+4	I(OH) =	21.7 mA

AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: TOTAL DOSE - 50 KRADS (Si) NO. OF DEVICES: 6

TEST NO.	INPUT	OUT1 (ns):	tPd0	tPd1	OUT2 (ns):	tPd0	tPd1
1	D0	Y0	33.8	31.3	Y3	33.8	34.7
2	D3	G'	20.7	20.0	OVR	34.2	33.7
3	Cn	RAM0	42.8	30.2	RAM0	.0	.0
4	I0	Y1	33.2	31.3	F3	39.7	27.8
5	I0	G'	19.8	29.0	OVR	48.7	38.5
6	D0	RAM0	44.5	36.2	RAM0	.0	.0
7	I5	Y0	27.0	19.3	Y2	21.7	13.7
8	I5	RAM0	42.5	24.2	RAM0	.0	.0
9	I5	Cn+4	32.2	34.0	Cn+4	.0	.0
10	I4	F=0	35.5	61.0	F3	38.2	25.7
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	19.0	16.7	RAM3	16.8	16.7
13	CLK	Q0	16.0	28.5	RAM0	49.3	56.3
14	CLK	Y0	33.8	38.3	Y0	33.8	38.3
15	CLK	Cn+4	44.7	54.5	Cn+4	44.7	54.5
16	A0	Y0	26.5	31.3	Y2	20.5	28.3
17	A3	Y1	21.7	31.0	Y3	21.3	30.0
18	B0	Y0	53.3	47.7	P'	49.7	32.7
19	A0	Y2	41.5	49.0	Cn+4	46.0	51.2
20	B2	G'	47.0	37.2	OVR	54.0	58.0
21	A2	G'	42.7	30.5	OVR	46.8	52.3
22	Cn	OVR	22.5	18.2	OVR	.0	.0
23	Cn	Y0	30.5	26.3	Cn+4	23.7	16.7
24	I8	Y3	22.3	24.5	Y1	18.5	24.7
25	CLK	Y1	51.0	.0	F=0	.0	81.7
26	CLK	Y3	.0	52.5	F3	.0	53.0

POWER SUPPLY CURRENT (Icc) = 130.0 mA

OUTPUT SINK CURRENT : Y0 I(OL) = 27.9 mA Cn+4 I(OL) = 21.7 mA
OUTPUT SOURCE CURRENT: Y0 I(OH) = 22.4 mA Cn+4 I(OH) = 20.8 mA

AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: TOTAL DOSE - 100 KRADS (Si) NO. OF DEVICES: 6

TEST NO.	INPUT	OUT1 (ns):	tPd0	tPd1	OUT2 (ns):	tPd0	tPd1
1	D0	Y0	34.5	31.2	Y3	34.5	34.0
2	D3	G'	21.7	19.8	OVR	34.5	33.8
3	Cn	RAM0	44.0	30.0	RAM0	.0	.0
4	I0	Y1	33.5	30.5	F3	39.7	28.0
5	I0	G'	19.8	29.3	OVR	49.0	37.8
6	D0	RAM0	44.8	36.3	RAM0	.0	.0
7	I5	Y0	36.8	19.5	Y2	22.0	13.2
8	I5	RAM0	43.3	24.0	RAM0	.0	.0
9	I5	Cn+4	32.3	33.8	Cn+4	.0	.0
10	I4	F=0	37.0	61.3	F3	38.2	25.0
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	19.0	17.5	RAM3	16.0	17.5
13	CLK	Q0	16.8	29.5	RAM0	49.8	57.2
14	CLK	Y0	35.5	38.8	Y0	34.5	38.3
15	CLK	Cn+4	45.2	55.7	Cn+4	45.2	55.7
16	A0	Y0	26.7	33.7	Y2	20.5	29.5
17	A3	Y1	22.0	29.8	Y3	21.3	29.8
18	B0	Y0	58.2	47.8	P'	52.8	32.5
19	A0	Y2	38.5	48.3	Cn+4	46.0	51.3
20	B2	G'	47.8	37.5	OVR	54.5	58.5
21	A2	G'	40.5	30.8	OVR	47.3	52.5
22	Cn	OVR	22.6	17.8	OVR	.0	.0
23	Cn	Y0	30.5	24.3	Cn+4	23.3	16.5
24	I8	Y3	22.5	24.5	Y1	18.3	24.5
25	CLK	Y1	51.8	.0	F=0	.0	82.1
26	CLK	Y3	.0	52.8	F3	.0	54.2

POWER SUPPLY CURRENT (Icc) = 129.9 mA

OUTPUT SINK CURRENT :	Y0	I(OL) =	27.3 mA	Cn+4	I(OL) =	21.9 mA
OUTPUT SOURCE CURRENT:	Y0	I(OH) =	21.9 mA	Cn+4	I(OH) =	20.7 mA

AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: TOTAL DOSE - 300 KRADS (Si) NO. OF DEVICES: 6

TEST NO.	INPUT	OUT1 (ns):	tPd0	tPd1	OUT2 (ns):	tPd0	tPd1
1	D0	Y0	34.5	33.0	Y3	34.5	35.8
2	D3	G'	21.7	23.0	OVR	36.0	34.3
3	Cn	RAM0	45.2	31.5	RAM0	.0	.0
4	I0	Y1	34.5	33.3	F3	40.5	29.7
5	I0	G'	21.3	30.7	OVR	49.7	40.7
6	D0	RAM0	46.2	37.2	RAM0	.0	.0
7	I5	Y0	28.0	20.3	Y2	22.8	14.3
8	I5	RAM0	44.8	25.0	RAM0	.0	.0
9	I5	Cn+4	33.5	35.0	Cn+4	.0	.0
10	I4	F=0	38.0	64.3	F3	39.5	27.0
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	19.0	18.2	RAM3	15.8	18.2
13	CLK	Q0	17.8	30.0	RAM0	51.5	59.0
14	CLK	Y0	35.7	39.7	Y0	35.7	39.7
15	CLK	Cn+4	46.2	56.7	Cn+4	46.2	56.7
16	A0	Y0	27.0	36.0	Y2	21.0	31.8
17	A3	Y1	22.3	31.8	Y3	22.0	31.8
18	B0	Y0	60.3	49.2	P'	56.3	33.7
19	A0	Y2	37.7	47.7	Cn+4	46.8	55.7
20	B2	G'	49.8	38.3	OVR	55.7	60.8
21	A2	G'	45.2	30.3	OVR	47.0	55.7
22	Cn	OVR	23.2	18.7	OVR	.0	.0
23	Cn	Y0	31.2	28.8	Cn+4	23.5	17.7
24	I8	Y3	23.3	25.3	Y1	19.0	25.3
25	CLK	Y1	52.5	.0	F=0	.0	83.2
26	CLK	Y3	.0	53.7	F3	.0	54.7

POWER SUPPLY CURRENT (Icc) = 125.9 mA

OUTPUT SINK CURRENT : Y0 I(OL) = 27.2 mA Cn+4 I(OL) = 21.4 mA
OUTPUT SOURCE CURRENT: Y0 I(OH) = 21.8 mA Cn+4 I(OH) = 20.6 mA

AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: TOTAL DOSE - 700 KRADS (Si) NO. OF DEVICES: 6

TEST NO.	INPUT	OUT1 (ns):	tPd0	tPd1	OUT2 (ns):	tPd0	tPd1
1	D0	Y0	33.7	31.5	Y3	36.3	36.2
2	D3	G'	19.8	19.7	OVR	37.2	34.5
3	Cn	RAM0	42.8	31.8	RAM0	.0	.0
4	I0	Y1	33.0	31.5	F3	41.3	30.0
5	I0	G'	20.0	28.7	OVR	50.8	38.8
6	D0	RAM0	45.7	36.0	RAM0	.0	.0
7	I5	Y0	26.0	19.2	Y2	22.5	14.2
8	I5	RAM0	43.3	23.7	RAM0	.0	.0
9	I5	Cn+4	31.8	33.2	Cn+4	.0	.0
10	I4	F=0	36.5	64.2	F3	40.5	26.8
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	17.3	16.2	RAM3	16.7	16.3
13	CLK	Q0	15.8	28.5	RAM0	44.2	60.2
14	CLK	Y0	31.8	37.8	Y0	33.5	37.8
15	CLK	Cn+4	44.0	55.3	Cn+4	44.0	55.3
16	A0	Y0	25.2	34.3	Y2	21.0	32.3
17	A3	Y1	21.2	31.2	Y3	21.5	31.5
18	B0	Y0	60.0	47.3	P'	58.7	33.5
19	A0	Y2	36.0	44.5	Cn+4	43.5	55.7
20	B2	G'	49.3	36.0	OVR	56.3	62.3
21	A2	G'	44.3	28.5	OVR	48.2	56.0
22	Cn	OVR	21.8	17.3	OVR	.0	.0
23	Cn	Y0	29.3	26.2	Cn+4	20.8	14.3
24	I8	Y3	21.8	23.2	Y1	20.2	25.0
25	CLK	Y1	51.0	.0	F=0	.0	83.8
26	CLK	Y3	.0	51.8	F3	.0	56.5

POWER SUPPLY CURRENT (Icc) = 122.5 mA

OUTPUT SINK CURRENT :	Y0	I(OL) =	27.2 mA	Cn+4	I(OL) =	21.8 mA
OUTPUT SOURCE CURRENT:	Y0	I(OH) =	22.0 mA	Cn+4	I(OH) =	20.9 mA

AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: TOTAL DOSE - 500 KRADS (Si) NO. OF DEVICES: 6

TEST NO.	INPUT	OUT1 (ns):	tPd0	tPd1	OUT2 (ns):	tPd0	tPd1
1	D0	Y0	34.5	32.2	Y3	35.5	35.5
2	D3	G'	22.7	20.3	OVR	36.0	33.8
3	Cn	RAM0	45.5	30.8	RAM0	.0	.0
4	I0	Y1	28.8	32.7	F3	40.7	28.7
5	I0	G'	20.3	30.0	OVR	50.3	40.2
6	D0	RAM0	46.3	36.7	RAM0	.0	.0
7	I5	Y0	27.5	19.8	Y2	22.8	14.2
8	I5	RAM0	44.7	24.0	RAM0	.0	.0
9	I5	Cn+4	32.5	34.3	Cn+4	.0	.0
10	I4	F=0	37.3	64.0	F3	39.5	27.0
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	18.3	17.3	RAM3	15.2	17.3
13	CLK	Q0	22.8	29.3	RAM0	46.3	59.3
14	CLK	Y0	35.3	39.3	Y0	35.2	39.3
15	CLK	Cn+4	45.5	56.3	Cn+4	45.7	56.3
16	A0	Y0	26.3	34.7	Y2	20.8	31.0
17	A3	Y1	22.2	31.2	Y3	21.8	31.2
18	B0	Y0	59.8	48.3	P'	56.3	33.5
19	A0	Y2	36.5	46.3	Cn+4	44.5	53.8
20	B2	G'	49.8	37.3	OVR	55.8	61.2
21	A2	G'	44.7	30.0	OVR	48.0	55.5
22	Cn	OVR	22.5	18.3	OVR	.0	.0
23	Cn	Y0	30.3	27.2	Cn+4	24.2	17.0
24	I8	Y3	22.8	24.3	Y1	19.2	24.7
25	CLK	Y1	51.7	.0	F=0	.0	84.7
26	CLK	Y3	.0	52.7	F3	.0	55.3

POWER SUPPLY CURRENT (Icc) = 124.8 mA

OUTPUT SINK CURRENT : Y0 I(OL) = 27.4 mA Cn+4 I(OL) = 21.4 mA
OUTPUT SOURCE CURRENT: Y0 I(OH) = 22.4 mA Cn+4 I(OH) = 20.6 mA

AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: TOTAL DOSE - 1 MRAD (Si) NO. OF DEVICES: 6

TEST NO.	INPUT	OUT1 (ns):	tPd0	tPd1	OUT2 (ns):	tPd0	tPd1
1	D0	Y0	34.2	31.7	Y3	37.3	36.3
2	D3	G'	21.5	19.3	OVR	38.3	35.0
3	Cn	RAM0	46.8	31.0	RAM0	.0	.0
4	I0	Y1	34.2	32.2	F3	43.0	29.5
5	I0	G'	20.7	29.7	OVR	52.5	40.3
6	D0	RAM0	47.2	37.0	RAM0	.0	.0
7	I5	Y0	27.5	18.8	Y2	23.5	14.5
8	I5	RAM0	45.5	24.0	RAM0	.0	.0
9	I5	Cn+4	33.5	33.8	Cn+4	.0	.0
10	I4	F=0	39.2	65.7	F3	42.0	27.8
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	17.3	17.2	RAM3	16.3	17.2
13	CLK	Q0	33.3	28.2	RAM0	53.0	58.7
14	CLK	Y0	35.0	39.3	Y0	35.0	39.3
15	CLK	Cn+4	45.3	57.0	Cn+4	45.3	57.0
16	A0	Y0	27.8	35.8	Y2	21.8	33.7
17	A3	Y1	22.3	32.5	Y3	22.7	33.5
18	B0	Y0	61.3	48.3	P'	62.0	34.2
19	A0	Y2	38.2	45.8	Cn+4	44.2	56.8
20	B2	G'	52.7	37.0	OVR	58.3	63.7
21	A2	G'	46.0	28.3	OVR	49.2	57.7
22	Cn	OVR	23.0	17.8	OVR	.0	.0
23	Cn	Y0	31.0	26.2	Cn+4	24.8	19.2
24	I8	Y3	23.2	23.8	Y1	21.5	25.3
25	CLK	Y1	53.0	.0	F=0	.0	84.5
26	CLK	Y3	.0	53.0	F3	.0	57.3

POWER SUPPLY CURRENT (Icc) = 124.4 mA

OUTPUT SINK CURRENT : Y0 I(OL) = 25.9 mA Cn+4 I(OL) = 21.6 mA
OUTPUT SOURCE CURRENT: Y0 I(OH) = 20.9 mA Cn+4 I(OH) = 20.3 mA

AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: TOTAL DOSE - 3 MRADS (Si) NO. OF DEVICES: 6

TEST NO.	INPUT	OUT1 (ns):	tPd0	tPd1	OUT2 (ns):	tPd0	tPd1
1	D0	Y0	35.2	32.0	Y3	37.0	34.0
2	D3	G'	21.2	19.0	OVR	37.8	33.6
3	Cn	RAM0	48.2	32.0	RAM0	.0	.0
4	I0	Y1	34.6	33.6	F3	41.4	30.0
5	I0	G'	21.8	30.4	OVR	51.8	40.0
6	D0	RAM0	47.8	37.8	RAM0	.0	.0
7	I5	Y0	27.8	60.0	Y2	23.0	14.2
8	I5	RAM0	47.0	25.2	RAM0	.0	.0
9	I5	Cn+4	34.6	35.2	Cn+4	.0	.0
10	I4	F=0	39.2	67.4	F3	41.4	27.2
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	17.0	17.0	RAM3	15.0	17.0
13	CLK	Q0	16.2	29.2	RAM0	51.4	59.6
14	CLK	Y0	35.6	40.6	Y0	35.6	40.6
15	CLK	Cn+4	46.2	58.8	Cn+4	46.2	58.8
16	A0	Y0	26.2	38.4	Y2	21.0	31.4
17	A3	Y1	22.4	34.6	Y3	22.6	33.6
18	B0	Y0	66.4	49.4	P'	61.2	32.8
19	A0	Y2	40.8	45.4	Cn+4	41.8	55.4
20	B2	G'	54.4	38.2	OVR	57.8	63.8
21	A2	G'	48.2	29.4	OVR	49.0	57.2
22	Cn	OVR	23.2	17.6	OVR	.0	.0
23	Cn	Y0	31.8	27.6	Cn+4	25.2	17.8
24	I8	Y3	23.8	24.0	Y1	21.6	24.6
25	CLK	Y1	59.4	.0	F=0	.0	78.6
26	CLK	Y3	.0	54.4	F3	.0	55.8

POWER SUPPLY CURRENT (Icc) = 114.8 mA

OUTPUT SINK CURRENT :	Y0	I(OL) =	26.6 mA	Cn+4	I(OL) =	21.5 mA
OUTPUT SOURCE CURRENT:	Y0	I(OH) =	22.2 mA	Cn+4	I(OH) =	20.5 mA

AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: TOTAL DOSE - 6 MRADS (Si) NO. OF DEVICES: 4

TEST NO.	INPUT	OUT1 (ns):	tPd0	tPd1	OUT2 (ns):	tPd0	tPd1
1	D0	Y0	35.8	32.0	Y3	37.0	35.3
2	D3	G'	22.8	19.5	OVR	38.3	34.0
3	Cn	RAM0	47.3	31.8	RAM0	.0	.0
4	I0	Y1	34.3	34.0	F3	41.5	30.8
5	I0	G'	22.0	30.8	OVR	51.8	39.8
6	D0	RAM0	46.8	38.0	RAM0	.0	.0
7	I5	Y0	28.3	20.0	Y2	23.3	14.8
8	I5	RAM0	46.3	25.0	RAM0	.0	.0
9	I5	Cn+4	34.8	35.8	Cn+4	.0	.0
10	I4	F=0	38.5	70.3	F3	41.5	27.3
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	17.5	17.5	RAM3	15.3	17.5
13	CLK	Q0	16.0	29.3	RAM0	51.8	59.0
14	CLK	Y0	35.8	40.8	Y0	35.8	40.8
15	CLK	Cn+4	46.5	59.3	Cn+4	46.5	59.3
16	A0	Y0	25.5	38.0	Y2	20.5	33.5
17	A3	Y1	22.3	33.5	Y3	22.3	32.5
18	B0	Y0	65.3	48.5	P'	61.0	32.8
19	A0	Y2	36.5	44.8	Cn+4	42.3	58.5
20	B2	G'	54.5	38.5	OVR	57.8	64.3
21	A2	G'	49.0	29.8	OVR	48.8	58.3
22	Cn	OVR	23.8	17.5	OVR	.0	.0
23	Cn	Y0	32.0	27.3	Cn+4	25.8	18.0
24	I8	Y3	23.3	24.5	Y1	20.8	25.3
25	CLK	Y1	53.3	.0	F=0	.0	87.3
26	CLK	Y3	.0	54.0	F3	.0	55.3

POWER SUPPLY CURRENT (Icc) = 120.4 mA

OUTPUT SINK CURRENT :	Y0	I(OL) =	23.0 mA	Cn+4	I(OL) =	21.0 mA
OUTPUT SOURCE CURRENT:	Y0	I(OH) =	19.7 mA	Cn+4	I(OH) =	19.3 mA

AM2901A DYNAMIC MEASUREMENTS (AVERAGE)

RADIATION LEVEL: TOTAL DOSE - 9 MRADS (Si) NO. OF DEVICES: 3

TEST NO.	INPUT	OUT1 (ns):	tPd0	tPd1	OUT2 (ns):	tPd0	tPd1
1	D0	Y0	38.3	34.0	Y3	40.0	35.3
2	D3	G'	22.7	20.3	OVR	39.7	35.0
3	Cn	RAM0	48.7	32.7	RAM0	.0	.0
4	I0	Y1	34.7	35.0	F3	42.7	31.3
5	I0	G'	22.7	31.3	OVR	54.0	41.7
6	D0	RAM0	47.7	49.3	RAM0	.0	.0
7	I5	Y0	29.0	21.0	Y2	23.3	14.7
8	I5	RAM0	47.0	25.7	RAM0	.0	.0
9	I5	Cn+4	35.3	37.0	Cn+4	.0	.0
10	I4	F=0	39.0	74.0	F3	44.0	28.3
11	I7	Q3	.0	.0	RAM3	.0	.0
12	I7	Q3	18.0	18.7	RAM3	15.0	18.7
13	CLK	Q0	17.0	29.3	RAM0	54.0	60.3
14	CLK	Y0	37.0	42.3	Y0	37.0	42.3
15	CLK	Cn+4	47.3	60.0	Cn+4	47.3	60.0
16	A0	Y0	26.7	39.0	Y2	21.3	34.3
17	A3	Y1	23.3	35.0	Y3	22.7	34.0
18	B0	Y0	75.7	50.3	P'	71.0	33.7
19	A0	Y2	38.7	48.0	Cn+4	44.0	68.3
20	B2	G'	56.7	39.3	OVR	61.0	67.7
21	A2	G'	50.0	31.7	OVR	53.0	61.3
22	Cn	OVR	24.7	18.7	OVR	.0	.0
23	Cn	Y0	33.7	28.3	Cn+4	25.7	19.0
24	I8	Y3	25.0	25.0	Y1	22.0	26.0
25	CLK	Y1	56.0	.0	F=0	.0	92.7
26	CLK	Y3	.0	55.3	F3	.0	57.0

POWER SUPPLY CURRENT (Icc) = 111.5 mA

OUTPUT SINK CURRENT : Y0 I(OL) = 24.2 mA Cn+4 I(OL) = 21.1 mA
OUTPUT SOURCE CURRENT: Y0 I(OH) = 20.2 mA Cn+4 I(OH) = 19.8 mA

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